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3-D COMPUTATIONAL SENSORS FOR ADVANCED LOW POWER VISUAL PROCESSING

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14. ABSTRACT
This report describes work performed in a collaborative effort between Northeastern University, MIT, and MIT Lincoln Laboratory to develop three-dimensional integrated circuit process technology and designs to enable advanced low power computational image sensors. The 3D development program was funded under DARPA contract DAAK60-96-K-0204 from June 4, 1996 through September 30, 2000. During the course of the program, over twenty people from these three institutions participated in circuit design, algorithm simulation, process development, modeling, and testing. The team produced six publications and three graduate theses. Lincoln Laboratory completed four full SOI/CMOS fabrication lots, along with multiple other shorter lots to verify different aspects of the process flow. Fifteen conventional CMOS chips were fabricated through the MOSIS service to test prototype designs, and a programmable demonstration camera system was developed to demonstrate the 3D imager and provide an environment for simulating future systems architectures.

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Preface

This report describes work performed in a collaborative effort between Northeastern University, Massachusetts Institute of Technology, and MIT Lincoln Laboratory to develop three-dimensional integrated circuit process technology and designs to enable advanced low power computational image sensors. The 3-D development program was funded under Defense Advanced Research Projects Agency contract DAAK60-96-K-0204 from June 4, 1996 through September 30, 2000.

We would like to acknowledge the support of Ellison C. (Dick) Urban of DARPA who funded this effort under the SMART MODULES program. Mr. Urban provided the guidance and vision to begin work on 3-D integration long before others recognized its importance to future technology development. We would also like to thank Henry Girolamo, Army Program Officer and Agent for DARPA at the Natick Soldier Systems Center, who provided the daily oversight and management of the program.

Summary

This report describes the development of 3-dimensional computational image sensor technology to allow high speed, high resolution image processing in compact low power portable systems. A major obstacle to building compact, low power systems for complex visual processing is the planar CMOS process. The restriction to two dimensions severely limits the type and number of concurrent communicating processors which can be placed on a single chip or linked across chip boundaries

The technology for fabricating 3-D sensors which has been developed is radically different from other 3-D integration approaches, which for the most part involve advanced packaging techniques, such as multi-chip modules (MCMs), and which require interconnect lines to be brought to the periphery of the chip stack. Our technology allows virtually unrestricted placement of vias connecting the stacked processing layers within the interior of the chip. Each pixel of the image acquisition layer is connected to an underlying processing element to perform massively parallel processing operations.

The 3-D process technology developed is based on standard processing of two-dimensional CMOS circuits on SOI wafers. The circuit layers are bonded together and interconnected through a post-CMOS process via fill and metallization. We have developed 3-D circuit designs for massively parallel image processing. One of the designs, for a 2-layer imager with pixel-parallel A/D conversion, was implemented in the 3-D fabrication process. Other designs, in particular one for an activity detection system, has been thoroughly simulated in software and may be implemented as a 3-D circuit in the future.

3-D COMPUTATIONAL SENSORS FOR ADVANCED LOW POWER VISUAL PROCESSING

1. Introduction

This report describes work performed in a collaborative effort between Northeastern University, MIT, and MIT Lincoln Laboratory to develop three-dimensional integrated circuit process technology and designs to enable advanced low power computational image sensors. The 3-D development program was funded under DARPA contract DAAK60-96-K-0204 from June 4, 1996 through September 30, 2000. During the course of the program, over twenty people from these three institutions participated in circuit design, algorithm simulation, process development, modeling, and testing. The team produced six publications and three graduate theses. Lincoln Laboratory completed four full SOI/CMOS fabrication lots, along with multiple other shorter lots to verify different aspects of the process flow. Fifteen conventional CMOS chips were fabricated through the MOSIS service to test prototype designs, and a programmable demonstration camera system was developed to demonstrate the 3-D imager and provide an environment for simulating future systems architectures.

Because of the scope of the tasks involved, this report is divided into four major sections. Section II describes the 3-D process technology development, which allowed the fabrication of the world's first functional 2-layer 3-D array image sensor with pixel-parallel A/D conversion. Section III discusses the architectural choices made in the sensor design and presents the theoretical performance limits of the 3-D sensor—over 100dB of dynamic range with less than 0.1% residual fixed pattern noise and 0.5% temporal noise. Section IV presents the results of the full range of tests made on fabricated devices—from process test structures to the 64x64 3-D image sensor array. Section V describes the programmable demonstration camera system and presents detailed simulations of an advanced algorithm based on the current pixel architecture for unusual activity detection. Finally, Section VI concludes with recommendations for future work to enhance the 3-D process to allow fabrication of high performance multi-layer circuits.

2. 3-D Process Development

The development of the active pixel sensor required advancement in three technological areas: low-power CMOS, photodiode sensors, and three-dimensional integrated circuit fabrication.

2.1. Low-power CMOS

2.1.1. 2-volt CMOS

The CMOS technology used to fabricate the CMOS circuits of the three-dimensional active pixel sensor had to be compatible with 5-volt operation and construction of three-dimensional integrated circuits (3-D IC's) composed of two active integrated circuits. The bulk CMOS technology used to fabricate the 3-D circuits was a modification of an internally funded program started at Lincoln Laboratory to establish a low-power CMOS capability in the Microelectronics Laboratory (MEL). The process, designed to operate at 2 volts with 0.4 volt thresholds, was developed using extensive process and device simulations and consisted of 10-nm gate oxides, dual-doped polysilicon gates, sidewall spacers, $TiSi_2$-cladded poly and source/drain regions, and RTP-activated junctions. The process utilized two levels of metal with the interlevel dielectric planarized by chemical-mechanical polishing. A 365-nm step and repeat lithography system with an effective field diameter of 2 mm was used for wafer processing. Functional 0.6-μm n and p-channel transistors and 0.8 and 1.2-μm inverters were obtained from the first run produced with the low-power process. Amplifiers with 0.8-μm gates, contacts, and vias were packaged upon completion of metal-2 processing and gains of 17 dB were measured at 1MHz, values consistent with Spice predictions. This bulk process was later scaled to 0.4-μm gate lengths and 0.6-μm contacts.

2.1.2. 5-volt CMOS

The operating voltage of the technology was extended to 5 volts by increasing the gate oxide thickness to 15 nm and by increasing the threshold voltages from 0.4 to 0.8 volts through modifications to the tub and channel implants doses. An improved salicide process that used $CoSi_2$ in place of $TiSi_2$, developed for a fully depleted SOI technology, was incorporated into the 5-volt CMOS technology. The CMOS circuits were fabricated using Silicon-on-Insulator (SOI) wafers as part of the three-dimensional fabrication process. The SOI wafers had a 1-μm buried oxide (BOX) and a 1-μm SOI layer. An outline of the photolithographic layers and key process steps and parameters is listed in Table 1 and the principal design rules are listed in Table 2.

2.2. Photodiode Process

The photosensors were fabricated in a 10-μm epi layer on a 0.3-μm BESOI layer with a 1-μm BOX. The epi thickness was chosen to optimize optical performance in the visible spectrum. Since the active pixel sensor would operate in the backside imaging mode, SOI wafers were used to aid in the 3-D assembly process as discussed below. The photosensors were fabricated with the same CMOS process as the circuit wafer.

2.3. Three-Dimensional Assembly Process

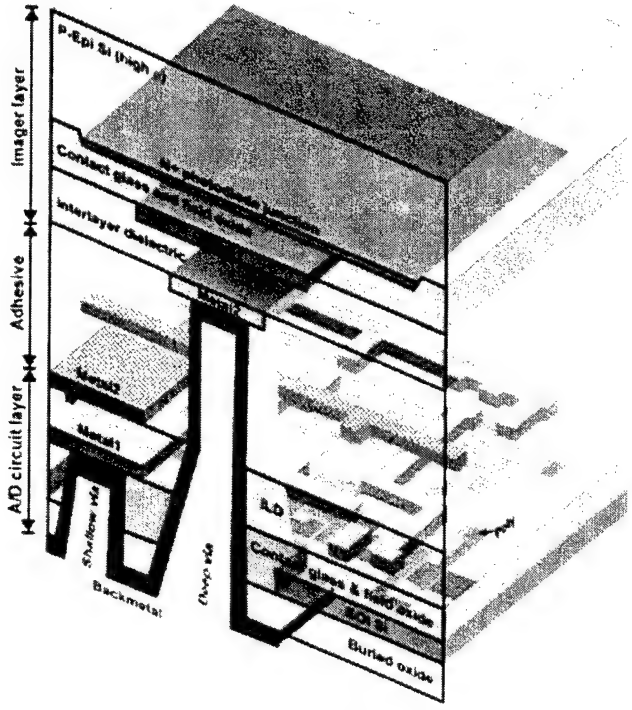


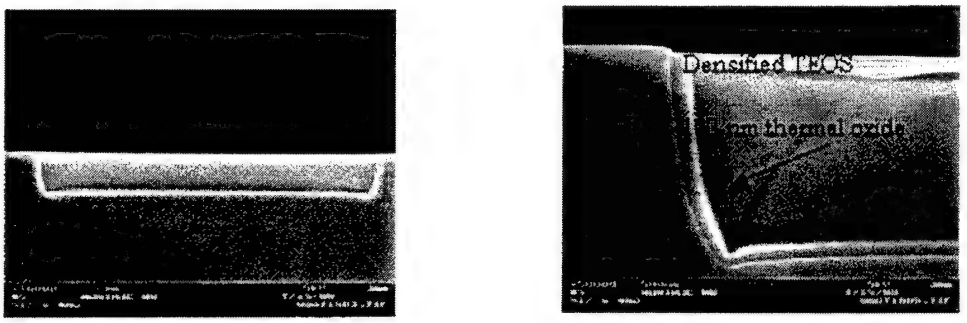
Figure 1. Conceptual view of deep and shallow 3-D via pair connecting two device layers.

The construction of a 3-D-IC consisted of bonding and interconnecting a SOI wafer with photodiodes to a SOI wafer with CMOS circuits. Prior to CMOS fabrication, Silicon trenches were etched through the SOI layer of the circuit wafer and filled with TEOS oxide to form channels through which 3-D vias would be etched to interconnect the two active layers. These vias are illustrated in Figure 1. After wafer fabrication and test, the circuit wafer was inverted, aligned to the sensor wafer, and bonded with a 3-μm adhesive. The bulk Silicon was then etched from the circuit wafer to expose the BOX. The BOX was used as a Silicon etch stop to produce a thin uniform active layer and is an essential step in the 3-D assembly technology. A set of

shallow 3-D vias was etched through the BOX, trench, and deposited oxides of the circuit wafer to expose metal pads on the first metal layer of the circuit wafer. A deep set of 3-D vias was defined and etched entirely through the circuit wafer plus the adhesive to expose metal pads on the second metal layer of the sensor wafer. The 3-D vias were 6-μm square and were 2.7 and 7.5-μm deep for the shallow and deep vias, respectively. An aluminum alloy was deposited and defined to connect the metal pads of the two wafers. The assembly was inverted and bonded to an oxidized Silicon wafer for mechanical support, and the handle Silicon was etched from the imager wafer to expose the epi layer for back side imaging. Bond pads were defined and etched through the BOX and 10-μm Silicon to expose pads on the first metal layer of the sensor wafer. The assembly was diced into chips and packaged; then the characteristics of active pixel sensors, ring oscillators, and test structures were determined. An outline of the key process steps in included in Appendix D.

2.4. 3-D Isolation

As discussed above, the 3-D interconnection process required that vias be formed through the circuit wafer so that connections could be made between metal-2 of the sensor wafer and metal-1 of the circuit wafer. An additional masking layer, 3-D Isolation, and a shallow trench isolation process was used to form the 3-D vias before initiating the conventional CMOS fabrication process. The process is outlined in Table 1 and a SEM of a 3-D via is shown in Figure 2.



(a) (b)

Figure 2. Scanning Electron Micrograph of 3-D isolation region in a bulk wafer.

Table 1. 0.8-μm CMOS process outline

(Basic steps are in bold face type)

Wafers	
Circuit Wafers	1-μm SOI on 1-μm BOX
Imager Wafers	10-μm SOI on 1-μm BOX
3-D Isolation	(Circuit wafers only)
Stress Relief Oxidation	15 nm
Nitride Deposition	200 nm
Photo-1: 3-D Isolation	
Plasma etch nitride, oxide, and SOI	
Trench Liner Oxidation	100 nm
TEOS Deposition	1350 nm
TEOS Densification	30 min at 950°C in nitrogen
CMP	Remove TEOS from nitride
Well Formation	
Initial Oxidation	15 nm
Photo-2: N-well	
N-well Implant	Phosphorus: 2.0x1012@200KeV
Photo-3: P-well	
P-well Implant	Boron: 1.5x1012@200KeV
Well Drive-in	20 min in oxygen+ 900 min in nitrogen at 1100°C
LOCOS Isolation	
Stress Relief Oxidation	36 nm
Nitride Deposition	1000 nm
Photo-4: Active	
Plasma Etch Nitride	
Photo-5: N-channel stop	
N-channel Stop Implant	Boron: 4x1013@75KeV
Photo-6: N-well	
P-channel Stop Implant	Phosphorus: 2x1012@50KeV
Field Oxide	450 nm
Channel Formation	
Sacrificial Oxidation	15 nm
Photo-7: N-channel Stop	
N-channel Implant	Boron: 5x1011@60KeV+ BF_2: 2.0x1012@60KeV
Photo-8: N-well	
P-channel Implant	Phosphorus: 1x1012@90KeV+ 1.2x10^{12}@40KeV
MOS Gate Formation	
Gate Oxidation	15 nm
Amorphous Silicon Deposition	225 nm
Photo-9: Poly	
Plasma Etch Amorphous Silicon	
Post Gate Etch Oxidation	15 nm
Source/Drain Formation	

Table 1. (Cont'd)

Photo-10: NIMP	
N-channel MDD Implant	Arsenic: 2.5x1014@75KeV
Photo-11: PIMP	
P-channel MDD Implant	BF_2: 5.0x1013@25KeV
Spacer	300-nm TEOS
Photo-12: NIMP	
N-channel Source/Drain Implant	Phosphorus: 3x1014@50KeV+ Arsenic: 5.0x1015@50KeV
Photo-13: PIMP	
P-channel Source/Drain Implant	BF_2: 5.0x1015@45KeV
Activation	30 s at 1000°C in 25% oxygen in nitrogen
Salicide Formation	
Metal Deposition	20-nm titanium on 8-nm cobalt
Silicide Activation and Etch	3 min in nitrogen at 550°C, etch in SC1 at 85C, 1 min in nitrogen at 700°C
Contacts	
LTO Deposition	Planarized 925-nm oxide deposited at 430°C
Photo-14: Contacts	
Plasma Etch Contacts	
Metal-1 Interconnect	
Contact Plug	Planarized 1030-nm Titanium Nitride/Titanium/Aluminum-Silicon Laminate
Metal-1 Deposition	630-nm Titanium/Aluminum-Silicon/Titanium/Titanium Nitride Laminate
Photo-15: Metal1	
Plasma etch Metal1	
Metal-2 Interconnect	
Interlevel Dielectric	650-nm planarized TEOS film plasma-deposited at 300°C
Photo-16: Via	
Plasma Etch Vias	
Via Plug	Planarized 1040-nm Titanium/Titanium Nitride/Titanium/Aluminum-Silicon Laminate
Metal-2 Deposition	630-nm Titanium/Aluminum-Silicon/Titanium/Titanium Nitride Laminate
Photo-17: Metal2	
Plasma Etch metal2	
Sinter	40 min at 400°C in 10% hydrogen in nitrogen

Table 2. 0.8-μm CMOS design rules

Feature	Min.	Min.
Well	10	6
3D Deep	6	25
Active	2.4	2.4
Polysilicon	0.8	1.2
Contact	0.8	0.8
Metal-1	1	1
Via	1	1
Metal-2	1	1

Contacts have a 0.8μm feature surround

Vias have a 1.0μm feature surround

2.5. In-process Oxide Measurements

Oxide thickness measurements of the field oxide and low temperature deposited oxide (LTO) were performed throughout the CMOS fabrication process using reflectance spectroscopy between 450 and 800 nm. Conventional reflectance thickness measurements assume a two-layer structure with Silicon as the bottom layer. Oxide measurements on circuit and imager wafers involve a four-layer structure—oxide, SOI, BOX, and Silicon—and are not reliable since small variations in the assumed SOI or BOX thickness can lead to apparent large variations in oxide thickness. Field oxide thickness measurements could not be reliably made on circuit wafers so the field oxide thickness was inferred from measurements of monitor wafers. Since there was no SOI in the 3-D Vias of the circuit wafers, we used the difference in two-layer oxide thickness measurements in the 3-D Vias before and after deposition to determine the LTO thickness. On sensor wafers, field and LTO oxide measurements were made by restricting the reflectance measurements from 450 to 650 nm since the 10-μm SOI layer of the imager wafers was sufficiently thick to absorb the light within that band.

3. 3-D Circuit Design

System architectures for real-time image processing can be categorized by their degree of parallelism at the sensor level, as shown schematically in Figures 3 through 5. At one extreme is the completely serial design in which pixels are read out sequentially from an imager, digitally converted by a single high-speed A/D, and stored in RAM for further processing. At the other extreme are fully parallel focal-plane processors, containing a processing element at each pixel. Column-parallel architectures, in which the pixels of a single column share a processor integrated on the same die as the sensor fall in between these two extremes.

The serial architecture can be implemented with or without integrating the A/D on the same chip as the imager. It is limited, however, in its ability to scale with speed and power. A 256x256 pixel imager operating at 30 frames per second requires a 2 Mega-sample per second A/D, while a 1Kx1K imager requires a 30 Mega-sample per second A/D for the same frame rate. At 1000 frames per second, these two imagers would need 65 Mega-sample per second and 1 Giga-sample per second A/Ds, respectively. Present limits on 8 bit low power converters are in the 40 Mega-sample per second range with 20-30mW of power dissipation. While low power A/D designs will certainly improve in the future, they will not scale proportionally with array size or frame rates. Serial output architectures will require multiple converters and consequently higher power dissipation and system complexity.

Column-parallel architectures require integration to achieve a high-bandwidth path between the sensor array and the processors. Since column processors operate at the row readout rate instead of at the pixel rate, the savings in power over a serial architecture can be substantial. To date, several area image sensors have been developed with column-parallel A/D conversion employing single-slope[1], successive approximation[2,3], and second-order current-mode Σ–Δ architectures[3]. Other examples of column-parallel processing include multi-resolution imaging[4], motion detection[5], computing the focus of expansion[6], and video compression[7]. In 2D technology, the area required for the processing circuits, which must be carefully laid out to match the column pitch of the sensor array, limits these designs.

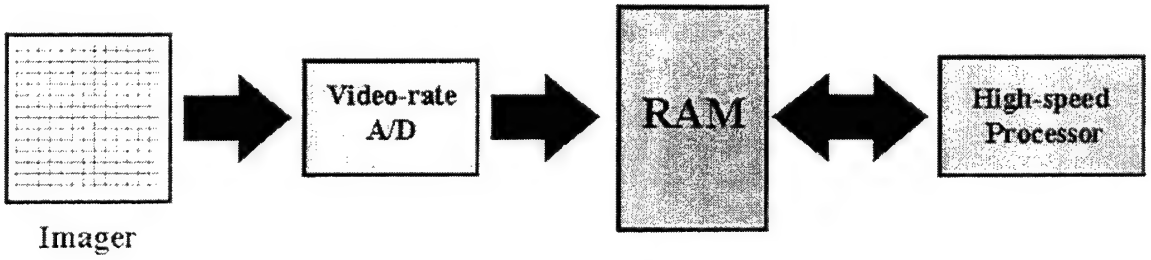


Figure 3. Serial readout with off-chip high-speed A/D.

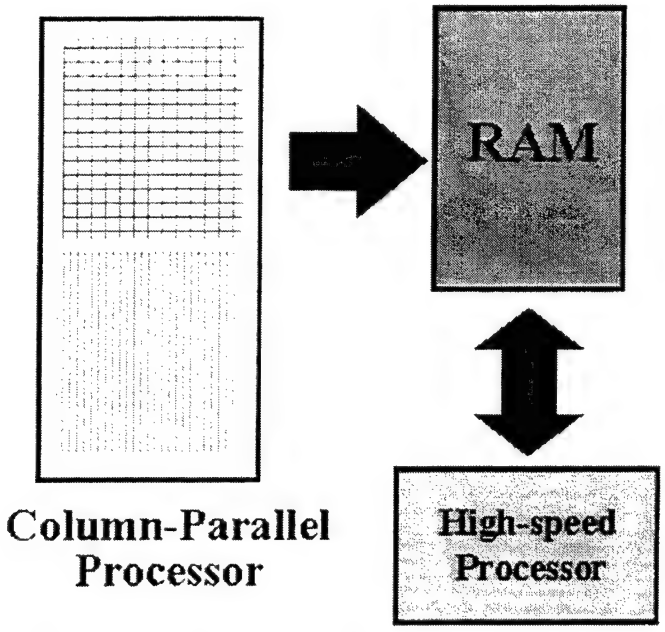


Figure 4. Column parallel on-chip processors.

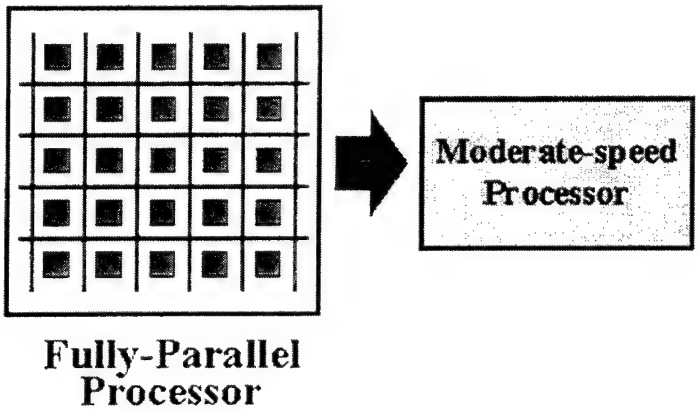


Figure 5. Fully parallel focal-plane processor.

Fully parallel architectures with one processor per pixel, or small group of pixels, have been implemented in 2D Silicon to perform specific image processing tasks such as edge detection, smoothing and motion detection[9,10], as well as for still imaging with analog-to-digital conversion[11,12]. The limited area available for the processing circuits imposes significant constraints on their complexity, however—even more so than with column-parallel architectures. As a result, most 2D focal-plane processors have been single-function low-resolution devices.

3-D technology provides enough bandwidth between the processor and sensor layers to accommodate complex fully- or block-parallel, architectures. The study undertaken in this program, which resulted in the development and implementation of fully parallel 3-D smart imagers based on first-order Σ–Δ pixel processors, was conducted in four stages:

- Analysis of active pixel architecture choices,
- Development of the theory behind processing first-order Σ–Δ output streams,
- Design, implementation, and characterization of the basic pixel-parallel A/D circuit as a 2D prototype, then as a 3-D array,
- Analysis of algorithms and architectures for multi-layer 3-D designs using the Σ–Δ A/D core

In the following sections, we will review the major findings and results from each major development stage.

3.1. Time-Based Active Pixel Sensors

Most CMOS active pixel image sensors are based on some variation on the 3T voltage-mode pixel shown in Figure 6. The photodiode node voltage is periodically reset to V_{rst}, and the photocurrent from the reverse-biased diode is integrated on the node capacitance for a fixed exposure time[13]. The final voltage is read by raising the select signal **SEL** to connect the source of M2 to the column bus, which is driven by a current source and acts as the output node of a source follower.

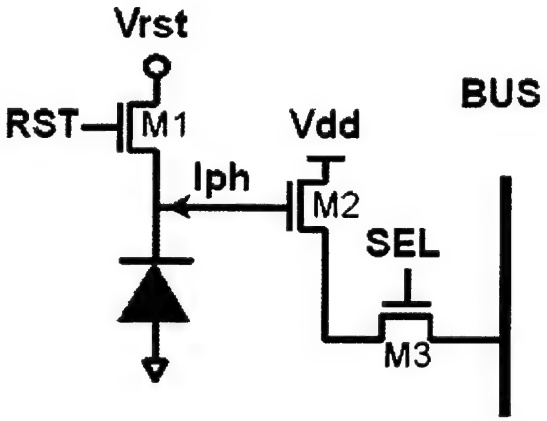


Figure 6. 3T Voltage-mode pixel schematic.

The primary problem with this design is the limited capacitance and voltage range available at the sensing node. With typical storage capacity of between 20 and 50Ke$^-$, photon shot noise by itself limits the resolution at the pixel to around 7 bits. Less than unity gain of the source follower can then consume another bit, leaving only 6 bits per pixel. As outdoor scene illuminations may contain over 5 orders of magnitude (100dB, or 17 bits) variation from the darkest to brightest objects, the limited signal-to-noise ratio of the voltage-mode pixel, as is, is unacceptable for photographic applications.

To overcome this problem, many designs have incorporated the use of time, in one form or another, as a control variable. Similarly to the voltage-mode pixel, the canonical "integration-

time"-mode pixel is depicted in Figure 7. In this case, the sense node is connected to a comparator which changes state when V_p goes below some reference value V_{low}. The state is reflected in the binary signal **OUT** that may be connected to an output bus and/or fed back to the reset transistor. If a global signal is used to reset the sense node to V_{rst}, the pixel operates as a timer. Conversely, if the loop is closed to connect the comparator output to the reset transistor, the pixel becomes an oscillator, which generates pulses on the **OUT** node at a frequency inversely related to the integration time.

One of the first imagers based on direct integration time measurement was the MAPP2200 sensor developed by Forcheimer *et al.*[1]. Later, Brajovic[14] introduced a modification to the direct timer architecture by assigning indices to pixels based on their relative switching times. This design allowed inherent gain control and histogram-based quantization, but was limited by its use of analog values to represent global quantities. Decker *et al*[15]. used a time-dependent barrier voltage to control the electron capacity of the integration node producing a non-linear illumination-to-voltage transfer curve. In the locally autoadaptive (LARS) imager developed by Silicon Vision GmbH[16], the integration time is measured in intervals, and a time-stamp voltage is stored in the pixel to record the number of intervals required to cross the reference level. In another design, D. Yang *et al*[17] used multiple sampling combined with pixel-parallel ADC to achieve wide dynamic range imaging. Their approach was to image the scene k times per frame at exponentially increasing exposure periods, T, ($2T$, ..., $2^k T$) digitizing the outputs at each exposure at low resolution (4-6 bits). By combining the values from each exposure at which the pixel did not saturate, a higher resolution m-bit value (m > 4-6) could be obtained. This value, together with the exponent of the longest non-saturating exposure period, gives a floating-point digital representation of the pixel illumination.

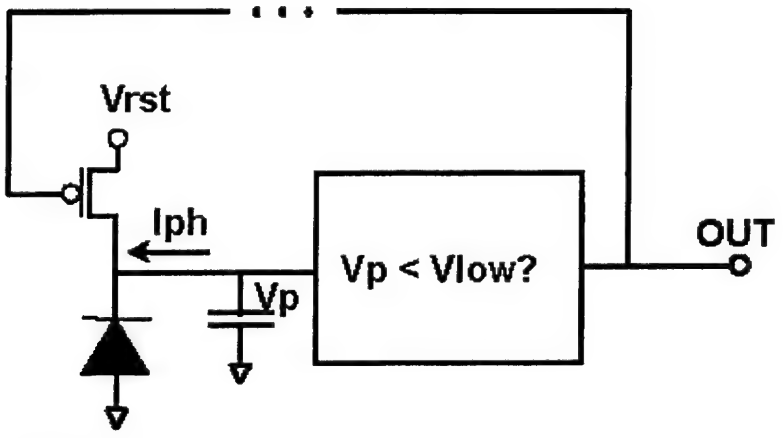


Figure 7. Canonical "integration time"-mode pixel schematic.

3.2. Asynchronous Σ–Δ Pixel Architecture

In choosing the design for the 3-D pixel, issues of circuit complexity, robustness, and noise immunity were weighed heavily along with issues of how the pixel processors could interact at a higher level—as they would need to in future multi-layer 3-D "smart" imagers. 3-D technology does not change the fact that the area per pixel is still limited. A 512x512 array fabricated on a 1 cm^2 die has less than 20μm x 20μm per pixel. However, as the readout rate of each pixel is very low—between a few tens of hertz to a few tens of kilohertz—the technology does offer the ability to trade off time for circuit complexity.

An oversampling Σ–Δ modulator architecture was thus chosen for the pixel processor because it does not require precision components—which would be impossible to achieve in such a small area—and because its output is a single bit stream which can be transmitted on a single wire. Despite the increased bandwidth that 3-D technology offers, having to maintain 8 or 10 wires per pixel for multi-bit operation would be an onerous burden. With an oversampling converter, the number of bits per pixel and the frame rate can be chosen to suit the demands of the application, and because it is also a "time-based" method, Σ–Δ conversion permits extremely wide dynamic range imaging. For the demonstration designs developed in this program for 2- and 3-layer 3-D fabrication, we implemented a first-order Σ–Δ converter with a free-running continuous oscillator sampled at fixed intervals.

Previous 2D imager designs with pixel-parallel Σ–Δ A/D conversion have been developed and demonstrated by Fowler and Yang[11,12]. These designs were based on a synchronous first-order Σ–Δ modulator containing a clocked comparator and a switched-capacitor circuit. The synchronous Σ–Δ system, depicted in Figure 8, is a discrete-time oscillator that fits into the canonical "integration-time"-mode depiction by adding a clock input to the box in Figure 7. A disadvantage to the synchronous modulator is that requires several analog components—a comparator, a 1-bit D/A, and a voltage summing operational amplifier—all of which contribute to fixed pattern noise and to design complexity. Furthermore, non-idealities in the analog circuits limit the maximum clock rate at which they may be operated, and in turn limit the achievable dynamic range.

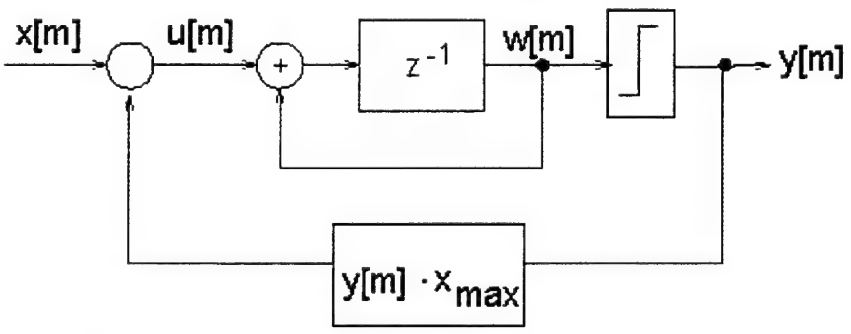


Figure 8. Block diagram of first-order Σ–Δ system.

In the design developed for the first 3-D imager, a continuous-time asynchronous sampled oscillator was used to create the Σ–Δ output stream. The pixel core contains a single comparator—its only analog component—and a pulse reset circuit. Instead of directly connecting the **OUT** signal, as it is called in Figure 7, to a bus, the information that it has switched state (or not) is stored on a MOS gate. This value is then read out and reset at a frequency determined by an external sampling clock. As reading this bit does not affect the oscillator, only the diode photocurrent determines the pixel frequency. It is thus possible to realize the full dynamic range allowed by the process technology.

3.3. Theory of First-Order Σ–Δ Modulation and Decoding

The equivalence between a synchronous first-order Σ–Δ modulator and a sampled oscillator running asynchronously with respect to the sampling clock is illustrated graphically in Figure 9. In the synchronous modulator, an input $x[m]$, generated by sampling the continuous quantity $x(t)$ at time $m\tau = m/f_s$, where f_s is the sampling frequency, is fed into an accumulator. If the accumulator output is above some threshold value, W_{ref}, the output $y[m]$ is set to 1 and a quantity x_{max} is subtracted from the next sample. If the accumulator output is below threshold, $y[m]$ is set to 0, and the next input sample passes unmodified to the accumulator. A typical waveform for a constant input $x(t)=c$ is shown as the solid staircase pattern in Figure 9. Next, consider a continuous-time circuit which integrates a constant input $x(t)=c$ until the accumulated value reaches the reference level W_{ref}. At this point the accumulator is reset to zero giving the sawtooth pattern. Clearly, given the same input, the continuous and discrete-time waveforms track each other. Furthermore, it can be observed that if the synchronous modulator crosses the threshold on a given clock edge m, then the equivalent asynchronous oscillator must have reset during the interval $((m-1)\tau, m\tau]$. Suppose now that the asynchronous circuit generates a pulse of width τ each time it resets and that this pulse is sampled on the next clock edge to generate the output, as shown in Figure 10. Setting the width of the pulse equal to the clock period guarantees that it will be sampled exactly once. As can be seen, the binary output streams from the sampled oscillator and the first-order modulator are the same.

It should be noted that sampling provides information only on the oscillator frequency. In the case of the sawtooth waveform shown, the frequency is proportional to the input and is the inverse of the time it takes to integrate from 0 to W_{ref}, or $T=W_{ref}/x$. If $T < \tau$, the output will saturate (all 1's) giving no further information. The maximum input which can be observed is thus $x_{max}=W_{ref}/\tau$, and the oscillator frequency can be expressed as:

$$f_{osc} = \frac{x}{x_{\max}} \cdot \tau \qquad (1)$$

The bit streams generated by each pixel must be decoded outside the imager array to produce digital numbers. Several techniques, ranging from convolution with FIR filters to linear programming methods, have been investigated for this purpose in other work[11]. In the course of this work, a new $O(N \log N)$ optimal algorithm was developed to decode first-order Σ–Δ sequences produced by a constant input[18]. This algorithm can be performed with fixed-point

arithmetic and, unlike $O(N)$ FIR filters, it does not require recomputing filter weights when the length of the bit stream changes. While a complete discussion of the algorithm and its underlying theory is outside the scope of this report, some of the key features of the algorithm are summarized below.

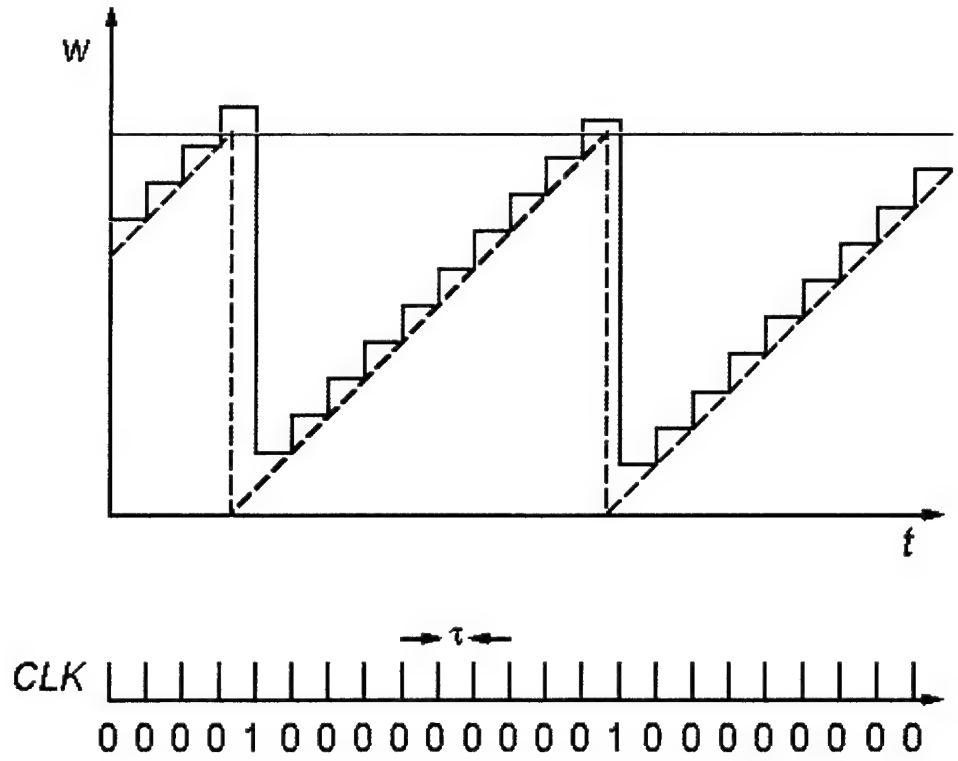


Figure 9. Waveforms of a synchronous S-D modulator (solid staircase) and an equivalent asynchronous oscillator (dashed sawtooth) based on a continuous integration of the input.

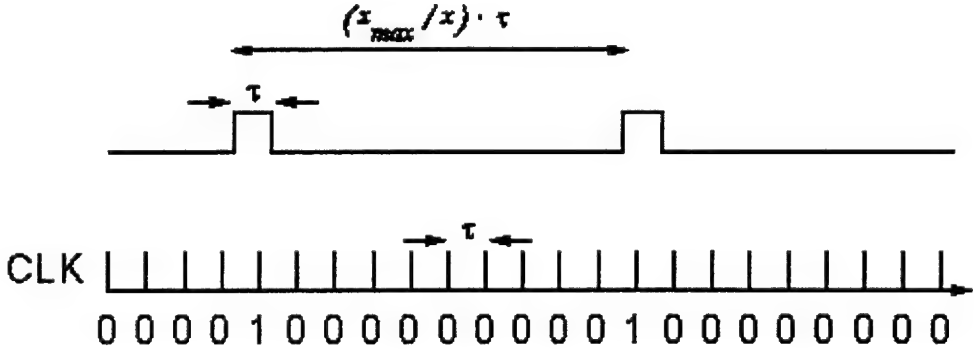


Figure 10. Periodic rectangular waveform generated by the asynchronous oscillator and the binary output from sampling at a rate $f_s=1/\tau$.

Average signal-to-noise ratio (SNR) vs. number of samples in the Σ–Δ output stream is plotted below in Figure 11 for the optimal decoder and for two FIR filters. The SNR is measured by computing the differences between the value computed by a particular decoding algorithm and the known value of the input that generated the bit stream. These differences were computed over a large sample set for inputs uniformly distributed over the range (0,1) and with randomly chosen initial states of the modulator. The mean squared error is computed as:

$$MSE = \frac{1}{M}\sum_{i=1}^{M}(x_i - \hat{x}_i)^2 \tag{2}$$

where $\hat{x}_i$ is the value computed for the stream generated by the ith input x_i, and M is the number of samples in the stream. The SNR is calculated from:

$$SNR = 10\log_{10}\frac{\overline{x^2}}{MSE} \tag{3}$$

As can be seen from Figure 11, the optimal decoder not only produces a roughly 4.2dB overall improvement in SNR, but has a slightly higher slope, 9.1 dB/octave, than the best FIR filter, which exhibits only 9 dB/octave. The number of bits of resolution in the digital output value is given by dividing the SNR in dB by 6. Hence the plot shows that for 6-bit resolution, approximately 20 samples are required, while for 8-bit resolution, approximately 48 are needed.

The new algorithm is also robust with respect to input noise, which for a pixel could arise from shot noise, dark current bursts, or FET noise in the input comparator, all of which would result in jitter in the oscillator frequency. Because of the regularity in the first-order Σ–Δ sequence patterns, very simple error correction techniques can be applied. Figure 12 shows the degradation of output vs. input SNR for the three methods and for 32 bit sequences. The input SNR is derived from the ratio of the mean squared signal to the mean squared phase noise. For these tests the magnitude of the phase noise was adjusted to result in a specified input SNR. The performance of the optimal decoder is superior to FIR methods down to 25dB input SNR.

For most video displays, 6 bits of resolution in the pixel values are adequate to display images without artifacts. However, the range of illumination levels in a typical scene may well extend over five orders of magnitude—*i.e.*, 100dB or 17 bits—between the brightest and dimmest features. It is important to point out that it is not necessary to decode each pixel to 100dB of resolution, which would require sampling over 400 bits per pixel, to cover the full dynamic range of the scene. The value determined by the Σ–Δ decoding algorithm is the ratio of the pixel oscillator frequency to the sampling frequency, f_s. It is sufficient to decode the pixel frequency to 6 bits of resolution with respect to the sampling frequency that it is most comparable to. This concept is equivalent to representing the values in floating-point notation, that is, with a mantissa and an exponent. The was applied by Yang *et al.*, in their floating-point pixel-level ADC image sensor[17], although the basis of their design was a voltage-mode pixel whose output was digitized after repeated exposures at binary-weighted integration times. The beauty of the sampled oscillator approach, unlike other Σ–Δ pixel designs, is that one can change the sampling frequency without perturbing the pixel oscillators. By sweeping through a set of

binary weighted frequencies, $f_s = f_0, f_0/2, \ldots, f_0/2^k$, and decoding only short-length sequences—*e.g.*, 8—16 bits—for each pixel, one can produce a high resolution floating-point output image over a very wide dynamic range.

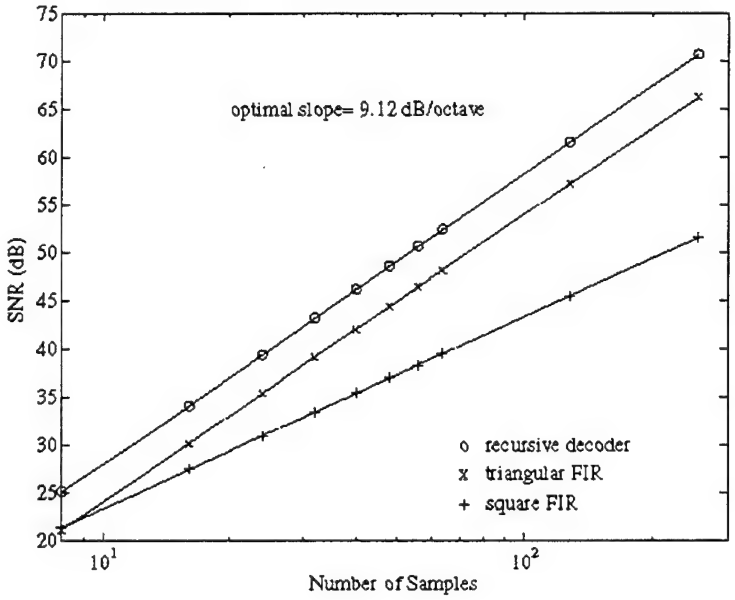


Figure 11. Comparison of average SNR as a function of number of samples for optimal decoder vs. triangular and square FIR filters.

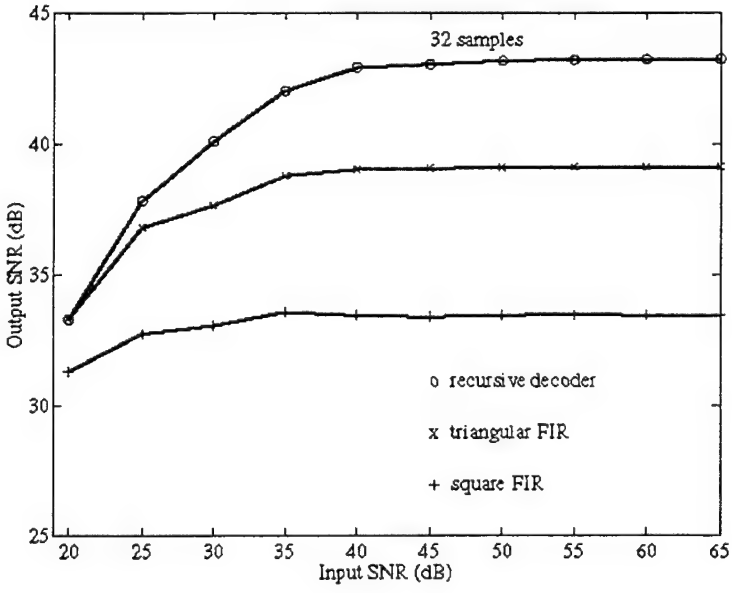


Figure 12. Degradation of SNR with input noise for different methods at sample size of 32 bits.

3.4. Asynchronous Σ–Δ Pixel Circuit Design and Characterization

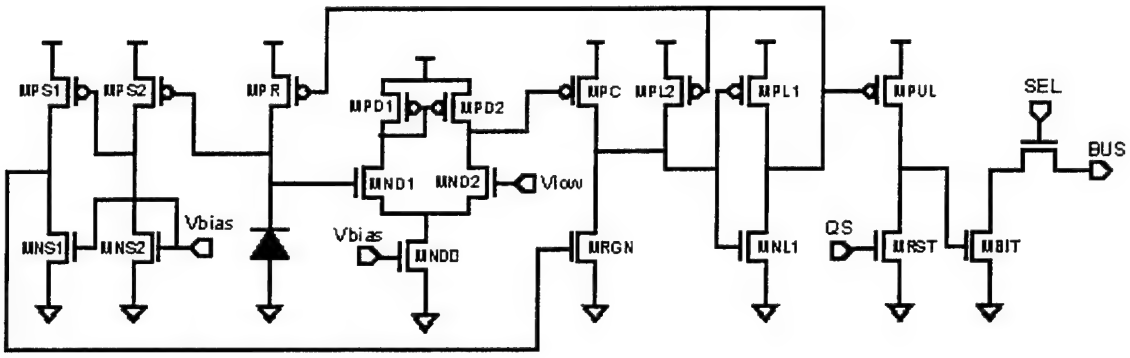


Figure 13. Σ–Δ converter cell schematic.

The schematic of the implemented asynchronous oscillator cell is shown in Figure 13. The input signal is the photocurrent generated by the n^+-p photodiode. The voltage on the integrating node decreases over time and is reset to V_{dd} when it drops below the global reference level, V_{low}. The circuit is composed of four sections: a differential amplifier, which continuously compares the photodiode voltage to V_{low}; a bistable half-latch which triggers the reset; a regenerative section that switches the bistable latch and restarts the integration; and pulse capture logic that stores a bit upon reset. The differential pair and the common-source amplifiers are biased in the weak inversion region to reduce power and maximize gain. A row select signal **SEL** gates the cell output onto a column bus in order to read the bit. Following the read, signal **QS** resets the storage bit to *GND*.

In order to confirm the predicted features of this circuit in an imager array, prototype cells were first fabricated through the MOSIS service in a standard 2D 3-metal 0.5 μm CMOS process. The photodiode was implemented on the same substrate as the oscillator circuit. Two imager arrays, one 48x48 array using patterned n-wells on the p-substrate for the photodiodes, and a 64x64 array with non-silicided n^+-diffusion on p-substrate photodiodes, were fabricated and tested. In both cases the unit cell, containing the oscillator circuit and the photodiode, measured 30μm x 30μm. The prototype imagers were characterized in the laboratory using a custom-built programmable test system. The camera test board provided the power supply and the reference voltages V_{bias} and V_{low}, set through programmable DACs, needed to operate the imager. Pixel output bit streams were stored in on-board SRAM and transferred to a PC via an EISA bus connector for decoding.

Data readout from the imager is performed by providing in sequence three pulsed signals for each row: bus precharge (**PC**), row select (**SEL**), and bit reset (**QS**). In order to minimize the possibility of losing a bit, the pulse width of these signals is kept short (< 100 ns) regardless of the row sampling rate. Rows are individually addressed, while columns are read out in parallel in groups of 16. For normal image acquisition, each row is read in order. Hence, if t_{row} is the time

required to read one row, and there are N rows in the array, the effective sampling frequency seen at each pixel is

$$f_s = \frac{1}{N \cdot t_{row}} \tag{4}$$

Sample raw images from each imager acquired with this test system are shown in Figure 14.

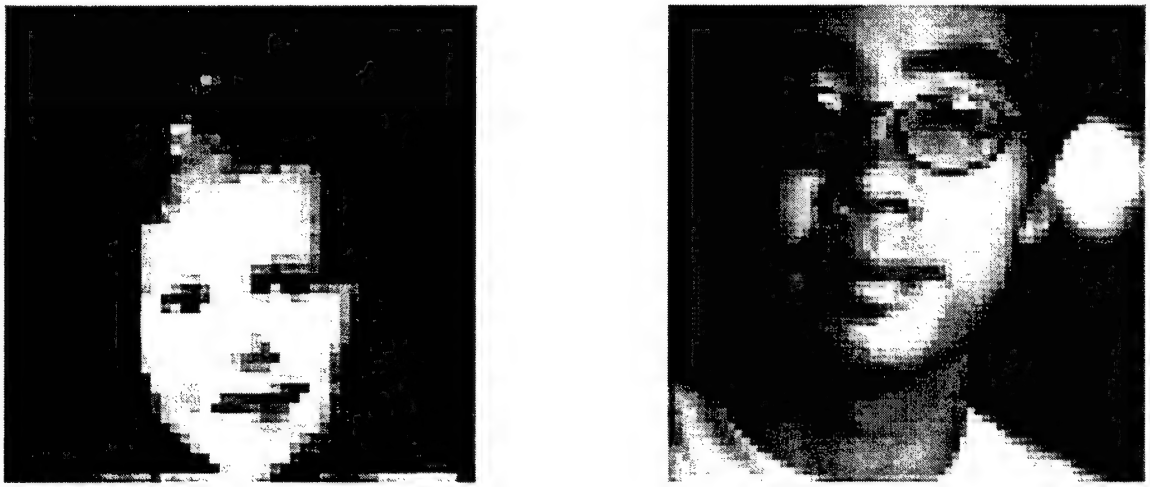


Figure 14. Sample images from prototype 2D devices—left: from 48x48 n-well diode array, right: from 64x64 non-silicided n-diffusion diode array.

The pixel bias current was nominally set at ~12nA, or 40nW power dissipation per pixel at V_{dd} = 3.3V by controlling the total average current drawn by the full array to be ~50 μA. As almost all on-chip processing, with the exception of the row and output select logic, is done in the pixel, this number essentially determines the total on-chip power dissipation. Extensive measurements were made to verify that exact bias current levels did not significantly impact the sensor performance. As seen from the data plotted in Figure 15, only modest variations—less than 2%—were observed at fixed illumination as V_{bias} varied from its nominal value to the point of strong inversion.

To determine the dynamic range of the sensor, the average output with respect to sampling rate was measured over a wide range of illuminations. The binary pixel output streams encode the ratio of the oscillator frequency to the sampling frequency $f_s = 1/\tau$:

$$\frac{x}{x_{\max}} = \frac{f_{pix}}{f_s} = \frac{I_{ph}}{C\Delta V}\tau \tag{5}$$

where I_{ph} is the photocurrent, $\Delta V = V_{\max} - V_{low}$, and C is the integrating node capacitance. Due to charge injection from the reset switch, V_{max} differs slightly from V_{dd}. For each of a set of clock frequencies from 305Hz to 156KHz, the light level was set to just saturate at the given

frequency, *i.e.*, $I_{ph}/C\Delta V = f_s$. It was clearly demonstrated that the pixel could oscillate at photocurrent-induced frequencies up to 156KHz before bandlimiting of the internal differential amplifier became apparent. The output with respect to sampling period was linear at all frequencies; further confirming that sampling did not affect the pixel frequency. Having determined the minimum sampling rate (~1 Hz) in the dark at which no response was measured due either to dark current or to transistor leakage, it could be ascertained that the effective dynamic range of the pixel oscillator was greater than 150000:1.

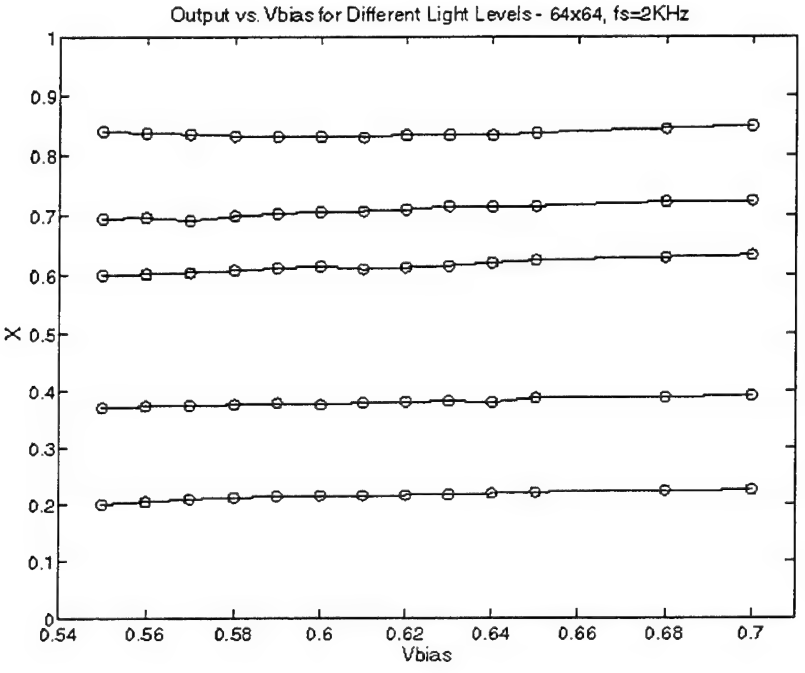


Figure 15. Output vs. Vbias for different light levels (64x64 array).

The pixel frequency can also be controlled through the global V_{low} parameter. Let $\alpha \equiv C(V_{\max} - V_{low})/(I_{ph}\,\tau)$ and $\tilde{x} \equiv x/x_{\max}$, then equation (5) can be rewritten as:

$$1/\tilde{x} = -\alpha V_{low} + \alpha V_{\max} \qquad (6)$$

A least-squares linear fit to a plot of $1/\tilde{x}$ vs. V_{low}, as shown on the left side of Figure 16, allows us to determine both α and V_{max}.

Spatial and temporal noise were measured by acquiring 32 sample images at each of several parameter settings. Temporal noise, computed as the average of the standard deviations of each pixel value across the 32 samples, was measured to be between 0.35% and 0.45% of signal for each sensor type. Repeated measurements of temporal noise while varying V_{low} and V_{bias} confirmed that it was uncorrelated with either of these parameters. It should be noted that correlated double sampling is unnecessary for the sampled oscillator pixels. Repeated sampling

of the integration time effectively reduces the noise due to the reset transistor by the square root of the number of resets in the sequence.

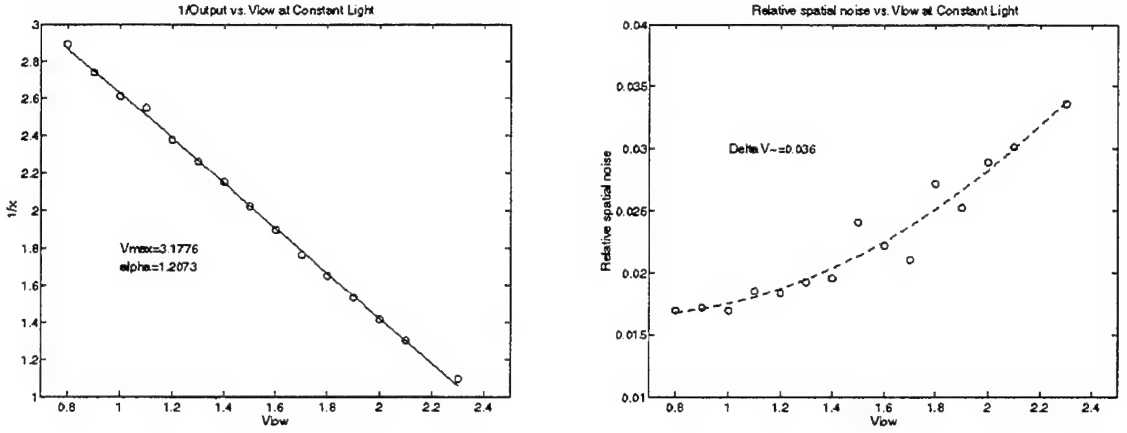


Figure 16. Inverse of output and standard deviation of relative spatial error vs. V_{low}.

Fixed pattern noise, defined as the standard deviation of array values from the array mean at constant illumination, was computed after averaging the 32 sample images to eliminate temporal variations. The raw fixed pattern noise relative to signal was found to be essentially independent of either V_{bias} or of the illumination, but was clearly related to V_{low}, as seen by the plot on the right of Figure 16. Referring to equation (6) and writing $\Delta V \equiv V_{\max} - V_{low}$ as $\Delta V = \overline{(\Delta V)} + \delta$, where $\overline{(\Delta V)}$ is the average value and δ the local variation, we obtain

$$\tilde{x} = \frac{1}{\alpha\overline{\Delta V} + \delta} \cong \frac{1}{\alpha\overline{\Delta V}}\left(1 - \frac{\delta}{\overline{\Delta V}}\right) \tag{7}$$

The standard deviation in $\tilde{x}$ is thus:

$$\sigma_x \cong \frac{1}{\alpha\overline{\Delta V}} \cdot \frac{\sigma_\delta}{\overline{\Delta V}} \tag{8}$$

where σ_δ is the standard deviation of ΔV, and the absolute error, $\sigma_x/\tilde{x}$, is thus $\cong \sigma_\delta/\overline{\Delta V}$. From a least-squares fit to the measured absolute error vs. V_{low}, it can be estimated that σ_δ is approximately 35-40mV across the array. While some of this variation may be accounted for by fixed differences in the average charge injected by the reset transistors, V_t mismatch in the comparators is most likely the primary source of fixed pattern noise.

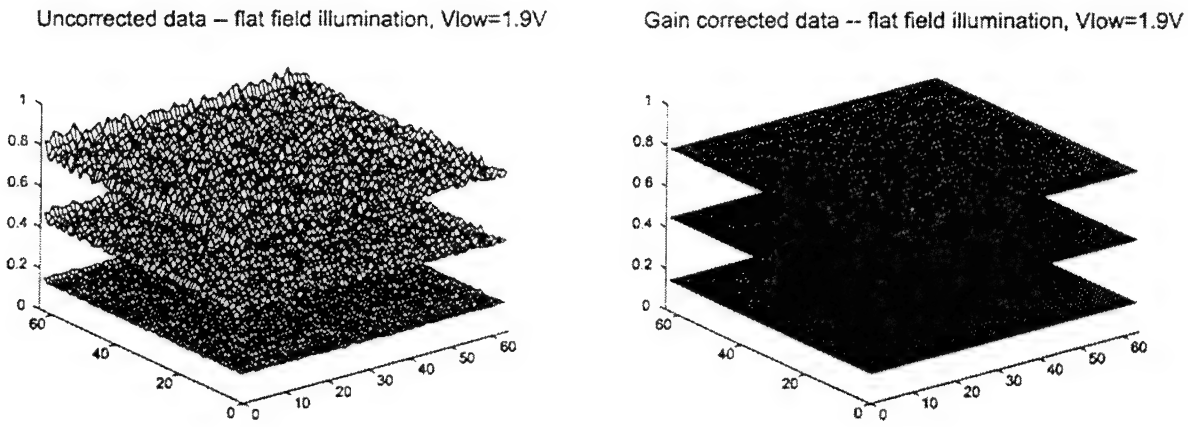


Figure 17. Flat field images from 64x64 2D sensor with and without fixed pattern noise correction.

The encouraging conclusion of these measurements is that the fixed pattern noise sources, whether due to reset transistor capacitance mismatch or V_t mismatch in the comparators, are relatively constant—*i.e.*, temperature- and illumination-independent properties of each cell—and are thus correctible. To make this point, the relative gain correction factors for the 64x64 array were computed for each pixel at a given V_{low} setting from a single image acquired under flat-field illumination. The left side of Figure 17 shows mesh plots of subsequent raw images taken at different illuminations, while on the right are shown the plots of the same images after multiplication with the computed correction factors. The residual relative fixed pattern noise after correction, measured over many illumination levels and V_{low} values, was measured to be approximately 0.1%.

4. Fabricated 3-D Circuit Characterization

Over the course of the program, MIT Lincoln Laboratory fabricated four device lots for two-layer 3-D circuits. These lots were identified as North1 through North4. North1, which was started in December 1997, was based on SOI process specifications derived at Northeastern University. North2 was the first lot fabricated with the Lincoln Laboratory-developed process and via isolation procedure described in Section II. The North2 mask set was used also for the North3 and North4 lots. The final lot, North4, was started after the completion of North2 and differed from the others in that bulk Silicon wafers, as opposed to the thick-epi SOI wafers, were used for the photodiode devices. The results reported on below are from devices fabricated in the North3 lot.

In order to save costs, a single mask set was used to process both the photosensor and circuit wafers. The "photosensor wafer" device layouts were mirrored within the *same* reticle as the "circuit wafer" layouts so that when the two wafers were physically aligned, with one facing the other, the appropriate devices on each layer would be matched together. A view of the mask set layout for the full reticle used in lots North2 through North4 is shown in Figure 18.

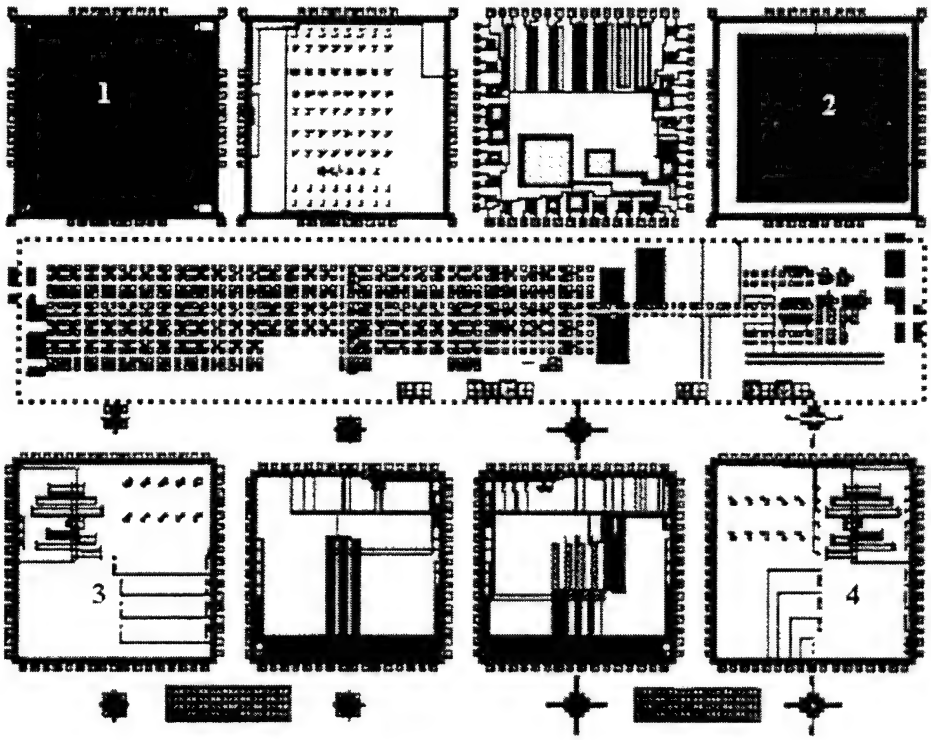


Figure 18. Depiction of mask set for runs North2-4.

4.1. 3-D Test Devices

4.1.1. Description of test structures

Test structures were designed and included in the reticle to characterize the CMOS and the 3-D interconnection processes. The active CMOS structures included n and p-channel transistors of variable gate widths and lengths to determine operational and isolation characteristics, inverters to measure output vs. input properties, and ring oscillators to measure transistor switching delay. The passive CMOS structures included polysilicon and metal structures to measure sheet resistance and determine the incidence of electrode shorts and opens and chains of contacts to measure metal-1 to Silicon, metal-1 to polysilicon and metal-1 to metal-2 resistance. Isolation structures were included to measure defects in the dielectric between polysilicon-Silicon, metal-1 to polysilicon, and metal-1 to metal-2. 3-D test structures included 3-D via chains of variable via sizes to measure yield and resistance and 3-D ring oscillators to determine the effect of the 3-D integration process on circuit delay. Photodiode test structures were included to measure diode leakage and to characterize the optical properties of devices in the normal and backside imaging modes. Diagrams of key test structures are shown in Figures 19 through 21. Originally, in the North1 lot, n-channel transistors without P-wells and n-channel depletion transistors were fabricated and tested. The process was modified in subsequent runs so those transistors became n-channel enhancement mode transistors with P-wells. The test descriptions were not altered.

The layout of a 3-D ring oscillator is shown in Figure 22. The arrows show how the inverters of the 3-D oscillators on each layer were paired so that the output of one on one layer connected to the input of another on the next layer. There were no complete conducting paths in the 3-D ring oscillators that did not pass through the 3-D vias. For comparison, 2D ring oscillators with equivalent numbers of stages were also laid out.

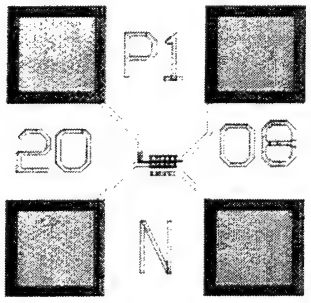


Figure 19. An n-channel transistor with a 20-μm gate width and a 0.8-μm gate length. The pad functions are: 1=gate, 2=source, 3= drain, and 4=body contact.

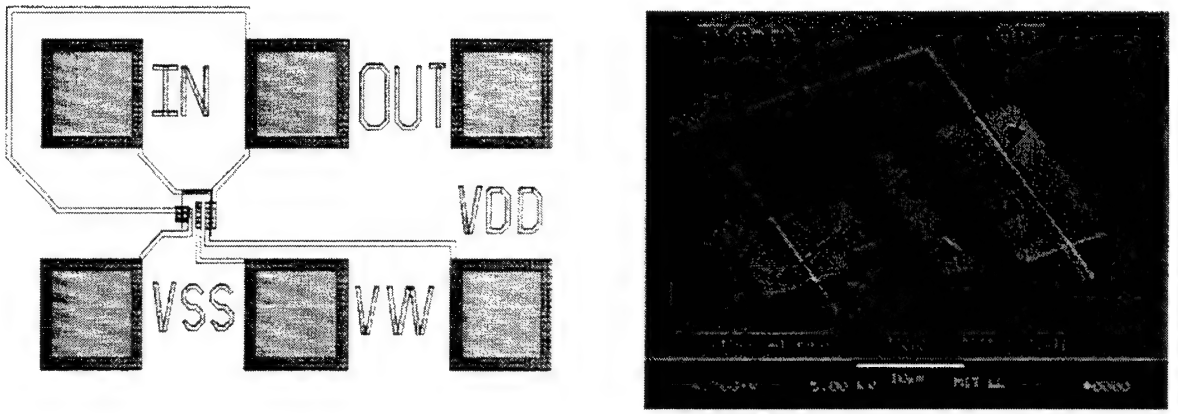


Figure 20. An inverter with a 0.8-μm gate length. The pad functions are shown adjacent to each pad in the drawing, (a). The SEM, (b), was taken after spacer formation and before metal-1 deposition.

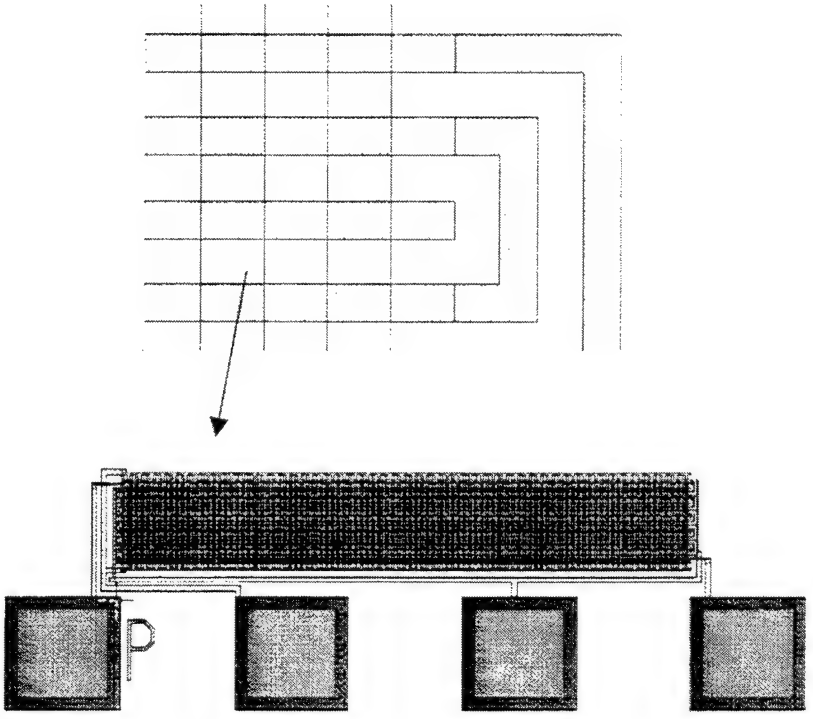


Figure 21. A polysilicon snake/comb structure over active used to detect gaps in polysilicon, shorts between polysilicon, and shorts between polysilicon and active. An expanded view in the upper figure shows a 1.2-μm poly line with 1.4-μm spaces (in blue) over 2-μm active features.

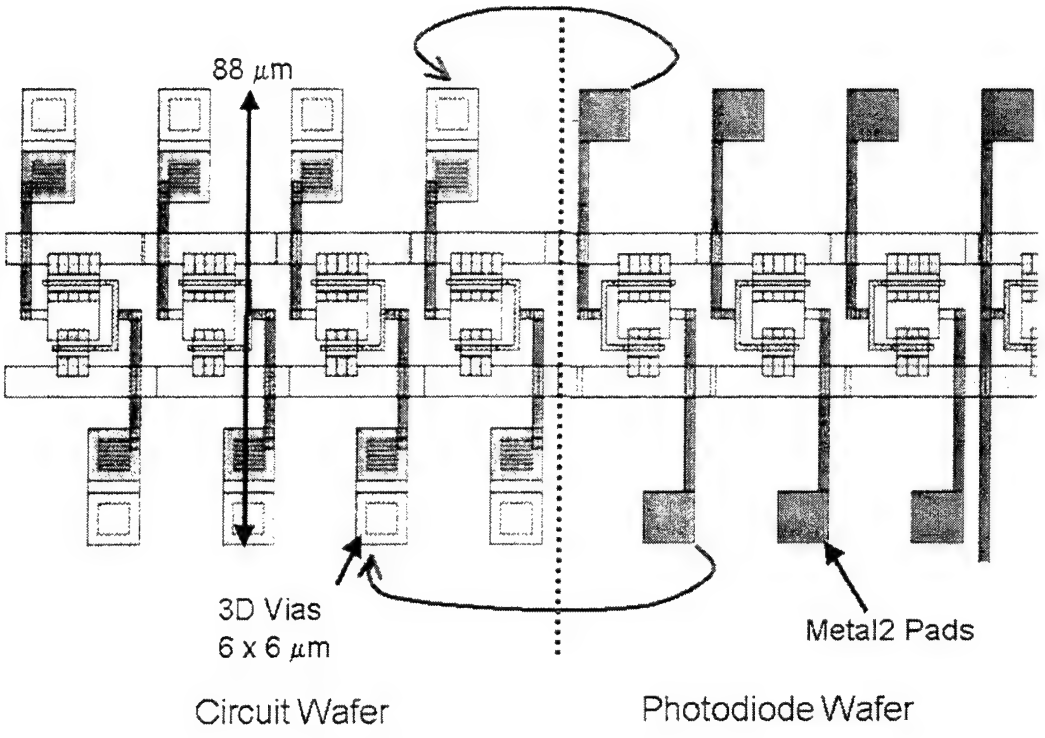


Figure 22. Layout of 3-D ring oscillator.

4.1.2. Tests performed

A limited set of active and passive CMOS measurements were performed at the conclusion of metal-1 fabrication to ensure that the fabrication process was in control. At the completion of wafer fabrication a complete set of tests was performed on approximately one-third of the wafers from each run. Over 200 active transistor measurements and 70 passive structural measurements were made per chip and 42 chips were tested per wafer. It had been observed that damage to metal probe pads as a result of testing could affect the epoxy bond integrity and lead to metal shorts through the bond. Thus wafers that were selected for 3-D integration were not tested but their properties were inferred from wafers from the same run that were tested. A description of the tests performed is listed in Appendix C.

4.1.3. SPICE Characterization

Transistors from the first 5-volt CMOS run were characterized using a parametric extraction program, BsimPro, to derive SPICE parameters for circuit design and simulation.

4.1.4. Data analysis

A summary of the key results from the process test devices of a typical wafer are listed in Table 3.

Table 3. Summary of Typical Wafer Test Data

Structure	Test	Yield	Median	StDev	Units
Nch-20x2-vt	71	100.0	0.597	0.00738	A
Nch-20x2-idl5	77	100.0	1.46E-10	1.61E-09	V
Nch-20x2-gm	81	100.0	4.70E-05	6.14E-07	S
Nch-20x.8-vt	85	100.0	0.586	0.008	V
Nch-20x.8-S	89	100.0	89.7	4.71	mV/decade
Nch-20x.8-idl5	91	100.0	1.45E-10	1.09E-09	A
Nch-20x.8-ids5	94	100.0	0.00741	8.08E-05	A
Nch-20x.8-gm	95	100.0	0.000125	3.14E-06	S
Nch-20x.6-vt	99	100.0	0.569	0.00636	V
Nch-20x.6-idl5	105	100.0	1.88E-10	1.64E-09	A
Nch-20x.6-gm	109	100.0	0.000171	5.91E-06	S
Ndep-20x2-vt	127	100.0	0.595	0.00728	V
Ndep-20x2-idl5	134	100.0	1.22E-10	3.09E-09	A
Ndep-20x2-gm	137	100.0	4.64E-05	5.72E-07	S
Ndep-20x.8-vt	141	100.0	0.583	0.00691	V
Ndep-20x.8-S	145	88.1	88.7	0.4	mV/decade
Ndep-20x.8-idl5	148	100.0	1.16E-10	2.25E-09	A
Ndep-20x.8-ids5	150	100.0	0.00741	7.34E-05	A
Ndep-20x.8-gm	151	100.0	0.000125	2.81E-06	S
Ndep-20x.6-vt	155	100.0	0.563	0.00809	V
Ndep-20x.6-idl5	162	100.0	1.17E-10	2.55E-09	A
Ndep-20x.6-gm	165	100.0	0.000167	4.44E-06	S
Pch-20x2-vt	183	100.0	-0.895	0.0053	V
Pch-20x2-idl5	189	100.0	-1.64E-10	1.39E-09	A
Pch-20x2-gm	193	100.0	1.11E-05	1.45E-07	S
Pch-20x.8-vt	197	100.0	-0.879	0.00481	V
Pch-20x.8-S	201	100.0	-105	3.89	mV/decade
Pch-20x.8-idl5	203	100.0	-1.61E-10	2.06E-09	A
Pch-20x.8-ids5	206	100.0	-0.0025	3.87E-05	A
Pch-20x.8-gm	207	100.0	2.69E-05	5.22E-07	S
Pch-20x.6-vt	211	100.0	-0.866	0.00516	V
Pch-20x.6-idl5	217	100.0	-1.66E-10	1.24E-09	A
Pch-20x.6-gm	221	100.0	3.50E-05	7.63E-07	S
Nch-2x.8-vt	253	100.0	0.742	0.0129	V
Nch-2x.8-idl5	259	100.0	1.35E-10	2.40E-09	A
Nch-2x.8-gm	264	100.0	0.000296	6.98E-06	S
Nch-.8x.8-vt	267	0.0			V
Nch-.8x.8-idl5	273	0.0			A
Nch-.8x.8-gm	277	0.0			S

Table 3. (Cont'd)

Structure	Test	Yield	Median	StDev	Units
Ndep-2x.8-vt	281	100.0	0.748	0.0135	V
Ndep-2x.8-idl5	288	100.0	1.08E-10	2.03E-09	A
Ndep-2x.8-gm	291	100.0	5.92E-06	2.36E-07	S
Ndep-.8x.8-vt	295	4.9	0.553	0.0488	V
Ndep-.8x.8-idl5	302	100.0	1.14E-10	1.56E-09	A
Ndep-.8x.8-gm	305	0.0			S
Pch-2x.8-vt	309	100.0	-0.912	0.0102	V
Pch-2x.8-idl5	315	100.0	-1.44E-10	2.77E-09	A
Pch-2x.8-gm	319	100.0	1.20E-06	4.40E-08	S
Pch-.8x.8-vt	323	0.0			V
Pch-.8x.8-idl5	329	0.0			A
Pch-.8x.8-gm	333	0.0			S
Isol-Nch	408	0.0	2.00E-10	2.18E-09	A
Isol-Pch	410	100.0	-1.56E-10	1.62E-09	A
Inv-low	413	100.0	-0.000155	7.00E-05	V
Inv-high	414	100.0	5	1.00E-02	V
PPly-Vt	416	97.6	-11.7	1.89	V
NPly-Vt	418	97.6	12	1.4	V
M1-N+SOI-Chn	475	100.0	1.52E+04	1.07E+03	Ω
M1-P+SOI-Chn	474	100.0	1.10E+04	583	Ω
M1-N+PLY-Chn	476	100.0	1.16E+04	989	Ω
M1-M2-Via-Chn	477	100.0	611	116	Ω
M1-N+-Rc	421	100.0	4.18	0.404	Ω
M1-P+-Rc	424	100.0	2.82	0.289	Ω
M1-Ply-Rc	427	100.0	3.29	0.428	Ω
M1-M2-Rc	430	100.0	0.528	0.216	Ω
Poly-snake	455	97.6	4.91E+04	3.72E+03	Ω
Metal1-snake	460	100.0	1.18E+03	44.3	Ω
Metal2-snake	465	100.0	222	4.56	Ω
Poly-comb@5V	457	97.6	-1.63E-10	1.61E-11	A
Metal1-comb	462	100.0	-1.57E-10	1.55E-11	A
Metal2-comb	467	83.3	-1.78E-10	5.44E-11	A
N+SOI-Rs	420	100.0	15.6	1.56	Ω/Sq
P+SOI-Rs	423	100.0	10.4	0.749	Ω/Sq
Poly-Rs	426	100.0	14.9	1.39	Ω/Sq
Metal1-Rs	429	100.0	0.0889	0.00359	Ω/Sq
Metal2-Rs	435	100.0	0.0751	0.00136	Ω/Sq
dLPLY	428	97.6	0.128	0.0694	µm
dLMetal1	431	100.0	-0.0426	0.038	µm
dLMetal2	437	100.0	-0.0305	0.0319	µm
M1-Ply-shorts	464	100.0	-1.97E-10	2.40E-11	A
M2-M1-shorts	469	97.6	-3.20E-10	1.94E-10	A

Table 4. Glossary of Symbols used in Table 3

Symbol	Description
vt	Threshold
idl5	Off-state Current
gm	Maxmimun
idl5	Drive Current
S	Subthreshold Swing
W	Gate Width
L	Gate Length

Associated with each test was a range of values that defined an acceptable result. The median and standard deviation were calculated for those parameters that were within the range and the yield was the percentage of values within the range. Note that the yields of .8x.8-μm transistors were very low. These devices had widths that were less than the design rule and were used to determine the effect of the LOCOS isolation process on the effective width of a transistor.

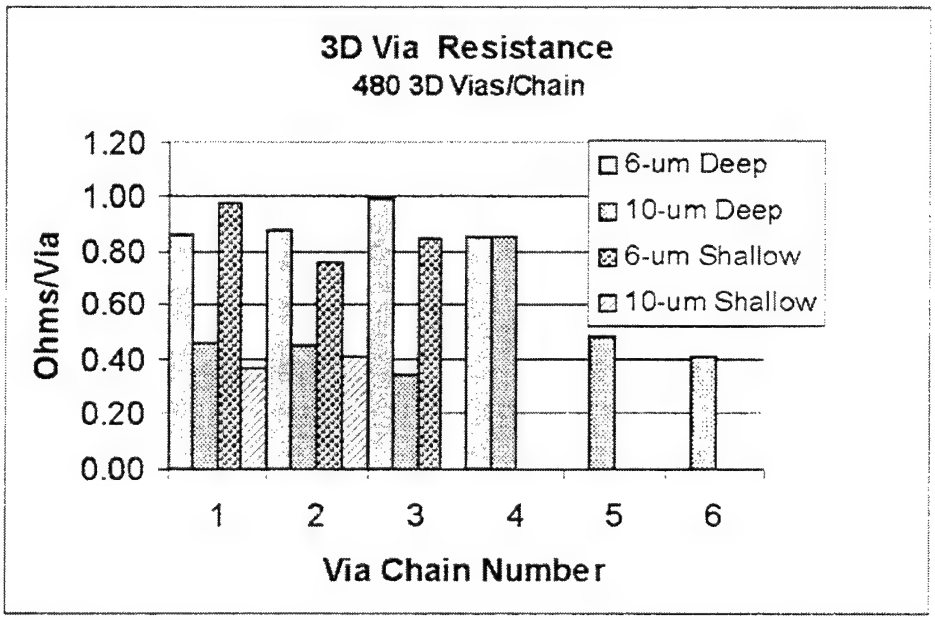


Figure 23. Measured 3-D via resistance from test chains.

The resistances of shallow and deep 3-D vias, graphed in Figure 23, were determined from measurements of the via chains, which each contained 480 vias in series. The median resistances of 10-μm square deep and shallow vias were 0.45Ω and 0.39Ω respectively, while the resistances of 6-μm square deep and shallow vias were 0.97Ω and 0.84Ω respectively. The equivalence of the deep and shallow via resistances indicates that etching through the epoxy did not degrade the contacts either by undercutting the bond layer or by contaminating the metal pads with adhesive residue. Via chains with 3-μm square deep and shallow vias were defective due to a reduction of the via contact area caused by shadowing during sputter cleaning. Although the yield was too

poor to give functional chains, there were nonetheless some functioning individual 3-μm via pairs. A scanning electron micrograph of one of these is shown in Figure 24.

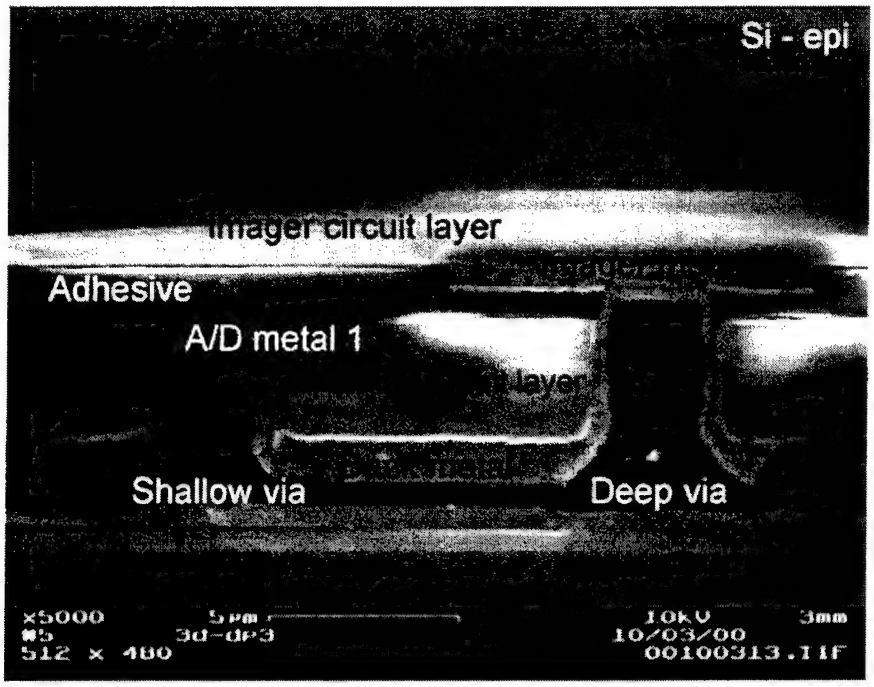


Figure 24. Scanning Electron Micrograph of functional 3μm via pair.

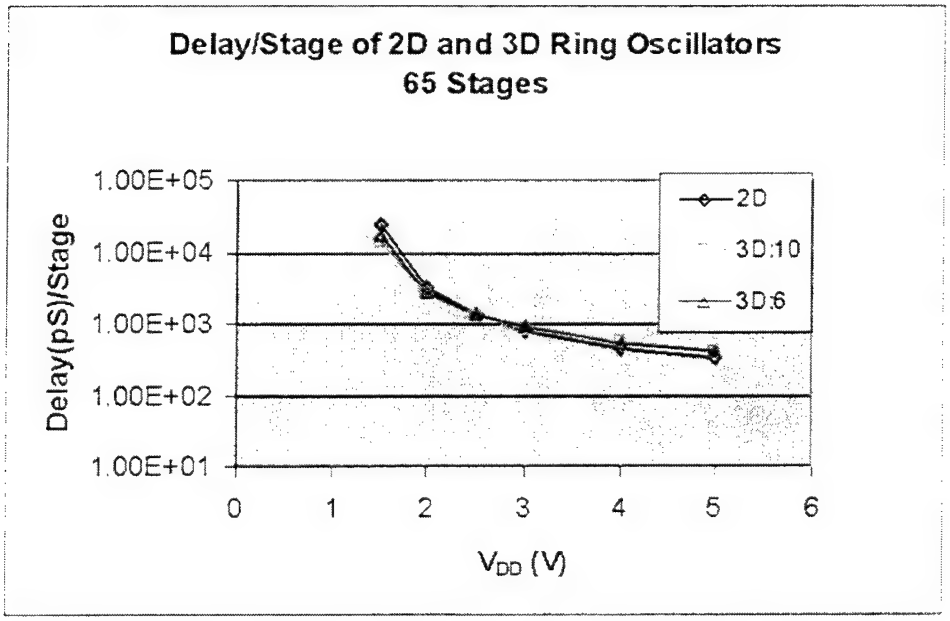


Figure 25. Measured delays per stage of 2D and 3-D ring oscillators.

As seen by the results plotted in Figure 25, the measured delays of the 2D and 3-D oscillators with 6 and 10-μm deep vias were equal, indicating the 3-D via design and fabrication process did not degrade the performance of the ring oscillators. Ring oscillators with 3-μm deep vias were included to determine the limits of the epoxy-bond process since the current design rules limited the deep via size to a minimum of 6 μm. These ring oscillator delays were characteristic of capacitively coupled vias, consistent with the model of most of the 3-μm deep vias being open.

4.2. Photodiode Characterization

An extensive study of the characteristics of photodiodes formed in the thick epitaxially grown Silicon layer on SOI wafers was performed. This analysis included developing a theoretical model of internal reflections from the oxide layers at the front and back of the epi layer. In addition, the model considered the effect of process parameters on the internal spectral response of the back-illuminated photodiodes.

For purposes of this analysis, some large area diodes were included on the North2 mask set. After fabrication, some selected epi wafers were bonded to blank wafers, and the handle was removed to expose the backside of the epi layer. The photodiode test devices did not contain any 3-D vias. However, etch cuts were made through the exposed backside of the bonded die in order to contact metal pads connecting to the test devices. Figure 26 shows the measured spectral response of a 400μm x 400μm test diode from the third fabrication lot (North3). The upper dashed-line curve depicts the ideal response that would result in perfect absorption given the internal reflections and resulting interference from the front and back oxide layers. The measured spectral response falls roughly 10% below the ideal curve. The calibration of the optical test system was verified using two light-emitting diodes (LED's) at known wavelengths in the green and red portions of the visible spectrum.

Given the calibrated measurements, it was then possible to estimate process-dependent parameters by modeling their effect on the spectral response. The three most critical parameters were: x_b, the thickness of a putative layer of traps at the SOI-epi interface, τ_n, the carrier lifetime in the material, and T_n, the recombination velocity. Figure 27 shows the least squares fit of the model to the measured data from variation of these parameters. The model curve fits the measurements very closely over most of the relevant spectrum and deviates only slightly at longer wavelengths in the height and position of the interference peaks. The maximum likelihood parameter values determined from fitting the model curve are given in Table 5. It is interesting to note that the value calculated for the interface trap layer thickness, $x_b = 7nm$, is very small, indicating that a dense layer of traps does not exist at the SOI-epi boundary. In addition the result suggests that the carrier mirror was correctly fabricated. The estimated carrier lifetime of $\tau_n \approx 150ns$ suggests that the density of defects within the epi layer is low.

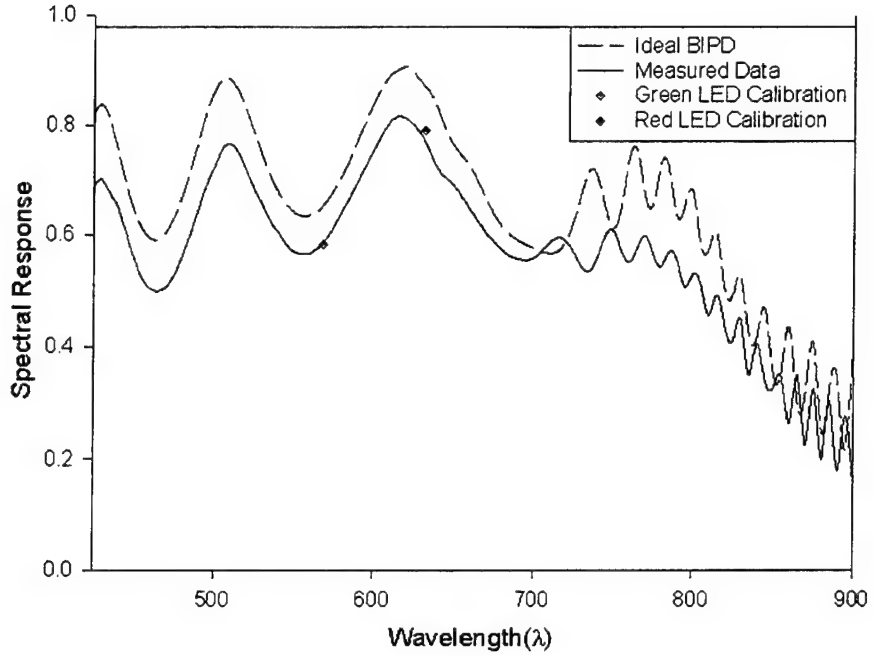


Figure 26. Measured results from 400μm x 400μm epi-layer test photodiode.

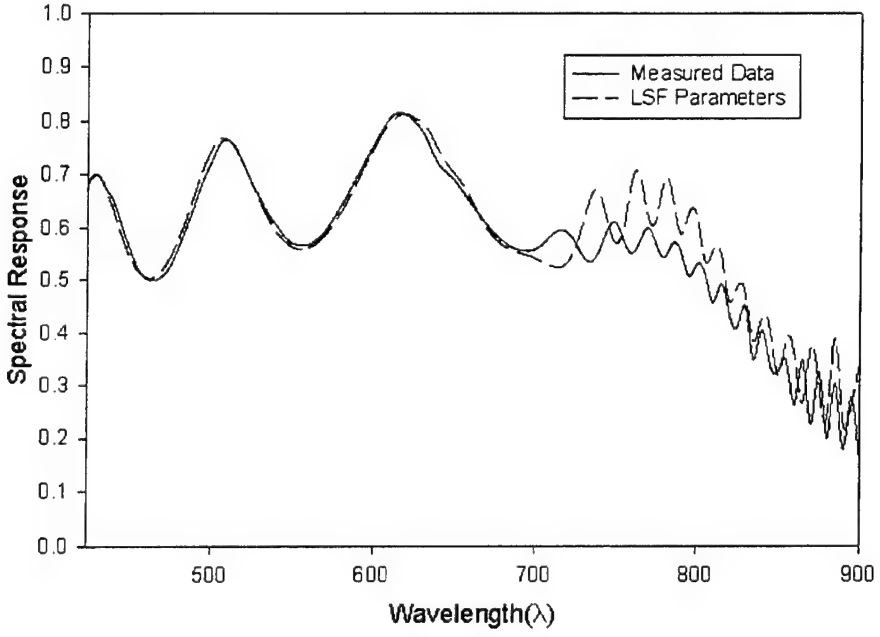


Figure 27. Least-squares error fit of model parameters to measured data.

Table 5. Determined Parameter Values

Fitting Parameters	Least-Squares Fitted Values
x_b	0.007μm
τ_n	1.457×10^{-7}s
T_n	6.409×10^{3}cm/s

4.3. 64x64 3-D Image Sensor with Pixel-Parallel A/D Conversion

The first-order Σ–Δ A/D converter pixel described in Section III was implemented as a 2-layer 3-D circuit by patterning a 64x64 photodiode array on the thick epi SOI wafer and a corresponding array of asynchronous oscillator cells on the thin film SOI wafer. The two arrays were designed such that when the completed wafers were aligned facing each other, each oscillator cell paired with a photodiode to which it was electrically connected through a 6μm deep and shallow via pair. The layouts for the pixel converter and the photodiode cells on each layer are shown in Figure 28. The active area (yellow rectangle in Figure) for the diode covers the entire pixel area, except for the 8μm gap separating it from the neighboring diodes. Because in the fully assembled imager, light is sensed through the back of the thick epi film, the metal pad which connects the active area to the deep via can be patterned over the surface of the diode without affecting its sensitivity. The 6μm vias were designed with a +/- 2μm surround to compensate for alignment tolerances. As can be seen, the resulting 10μm x 10μm areas required for each via on the circuit layer consume a large fraction of the total cell layout. Future technology development efforts should target reducing the via sizes to allow smaller pixels. For the layouts shown, designed for the 0.8μm SOI/CMOS process, each pixel measured 45μm x 45μm.

Some sample images taken with the 3-D sensor are shown in Figure 29. The overall picture quality is good; however, there are many anomalous pixels that are either too dark (below normal light response) or white (excessive light response). The causes of these anomalies have been determined to be either excessive leakage in the PFET reset transistor (cf. Figure 13)—which diminishes the effectiveness of the photocurrent in discharging the sense node—or high photodiode dark current—which will cause the pixel to saturate. Fortunately, fewer than 5% of all pixels were affected by one of these problems.

Further analyses of the imager characteristics under extremes of illumination and sampling rates revealed that all 4096 deep and shallow 3-D via pairs were functional. Figure 30 shows mesh plots of the array responses in total darkness at the maximum sampling rate, and in very bright light at the minimum sampling rate. The dark response (left) shows that only three pixels had such high dark current that they saturated at the highest sampling rate. All other pixels, however, did exhibit some measurable light response. The bright response (right) demonstrates that all pixels will saturate given enough light. Since there is no mechanism for discharging the sense node other than through the diode photocurrent, which passes through the 3-D via pair, this plot proves that all vias were conductive.

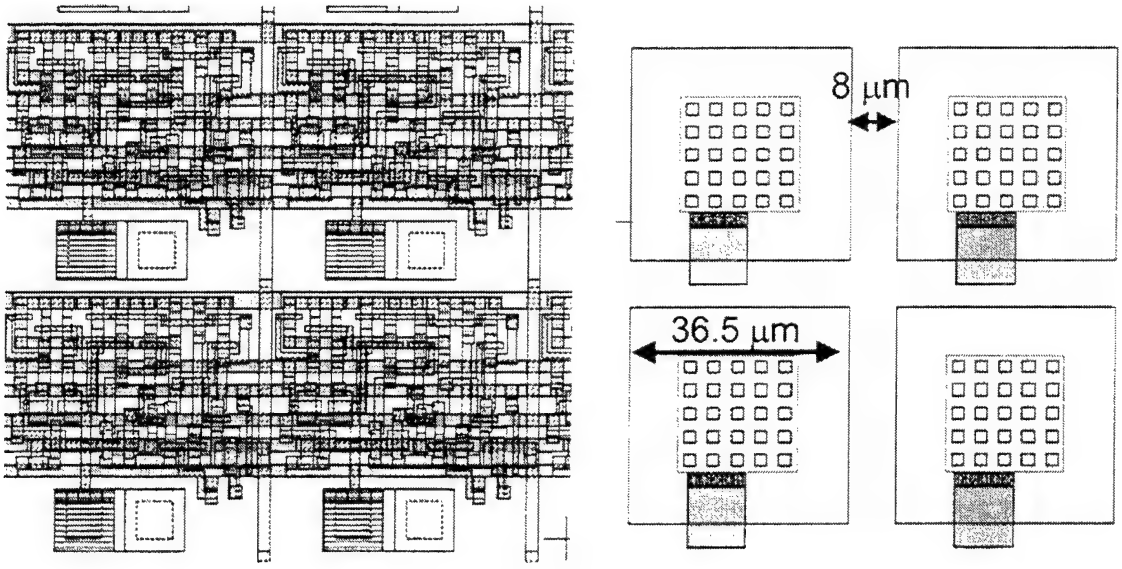


Figure 28. 3-D pixel layout.

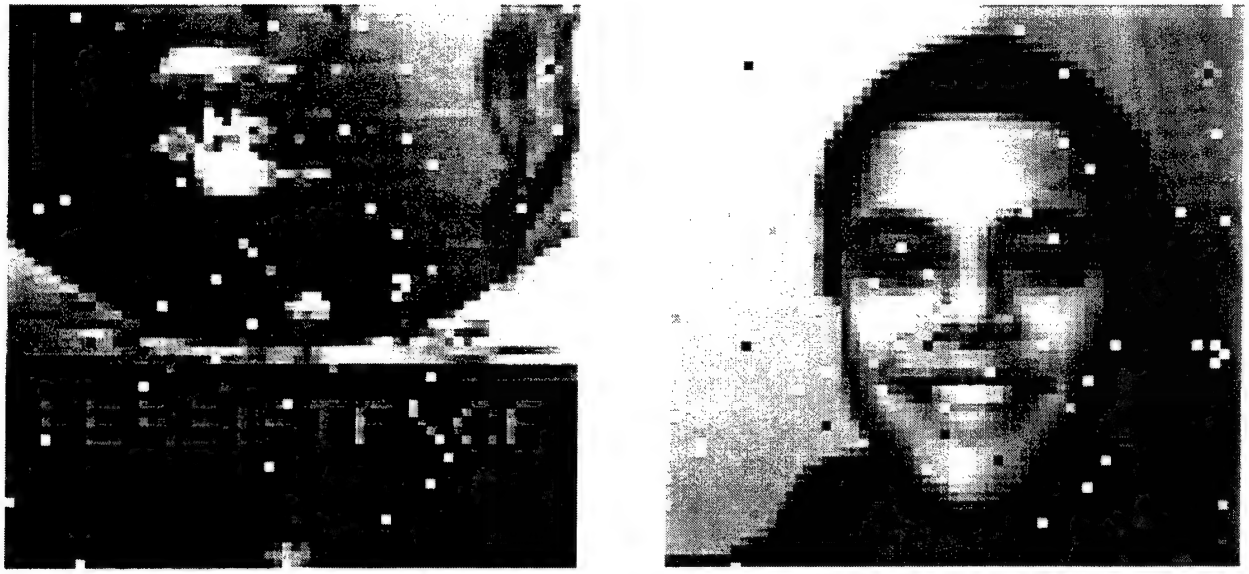


Figure 29. Unretouched sample images from 3-D 64x64 imager.

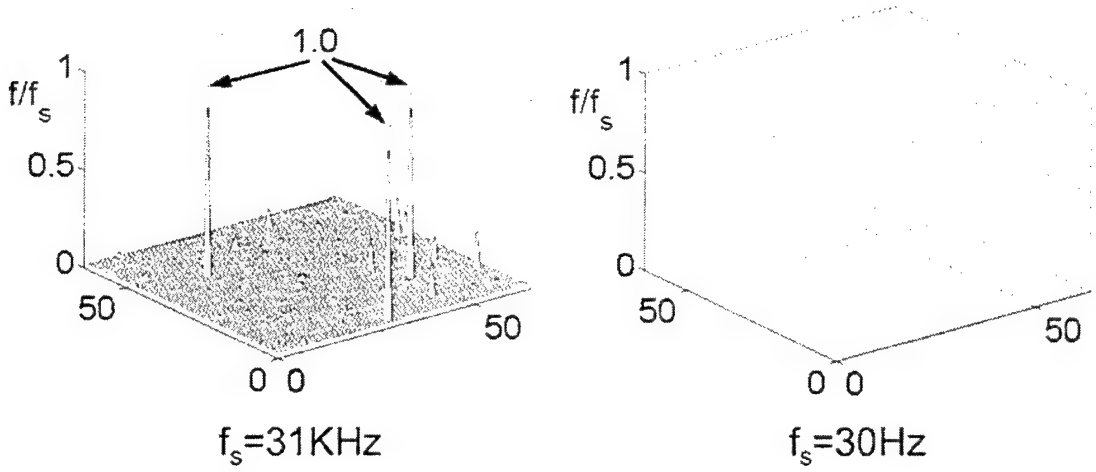


Figure 30. Performance of 3-D vias and process.

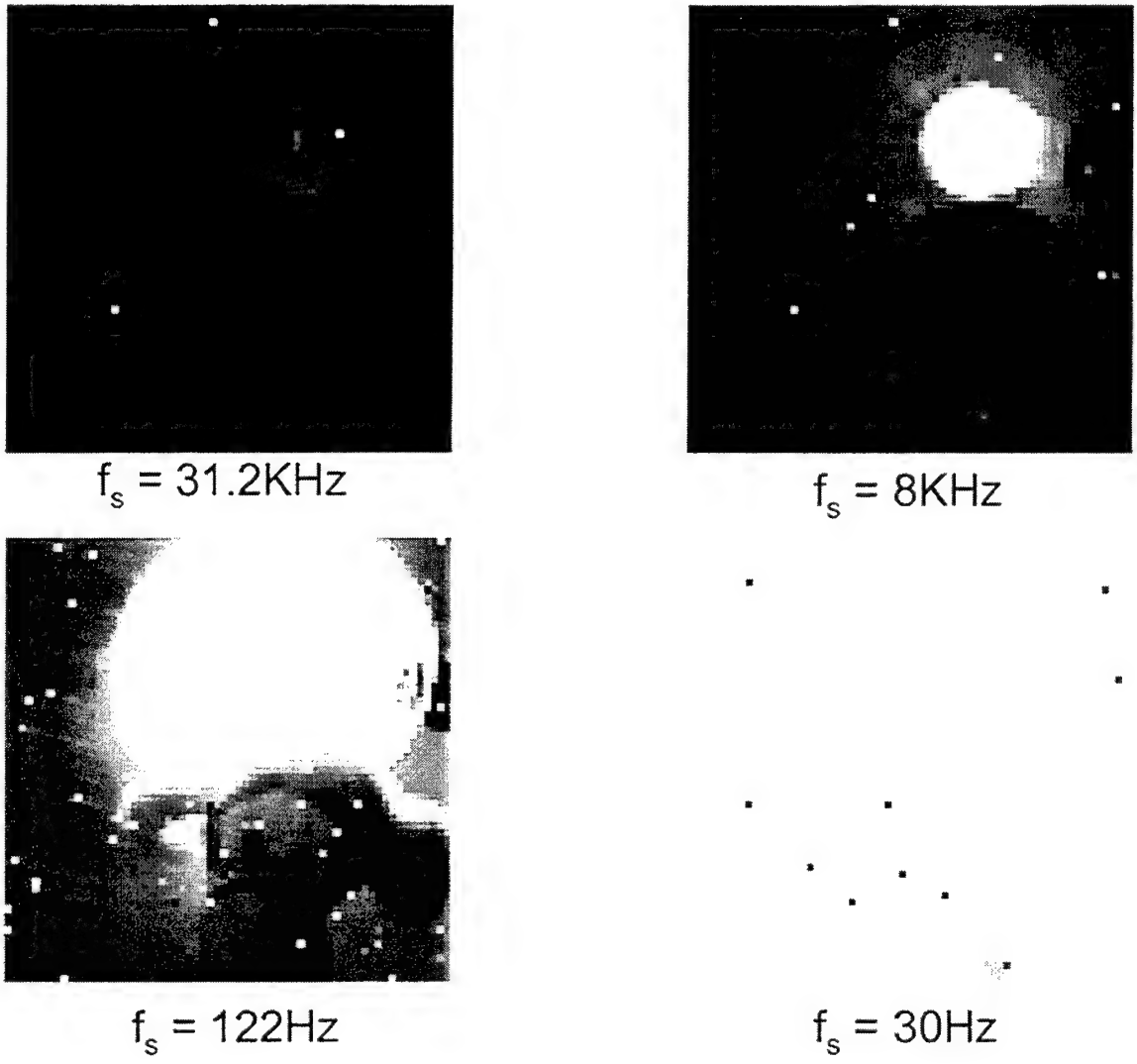


Figure 31. Dynamic range demonstration with full array.

Figure 31 illustrates the range of 3-D pixel responses that could be measured with the demonstration camera system. The four images shown were acquired at sampling frequencies varying from 30Hz to 31.2 KHz. Other than the sampling frequency, none of the scene or camera parameters was changed from image to image. The range of illuminations shown thus illustrates the actual range of oscillation frequencies of the pixels in the array. Only the clock speed limitations of the camera prevented us from sampling a full frame at higher frequencies to demonstrate the full dynamic range of the pixels.

5. Systems for Future Multilayer 3-D Devices

5.1.1. Demonstration Camera System

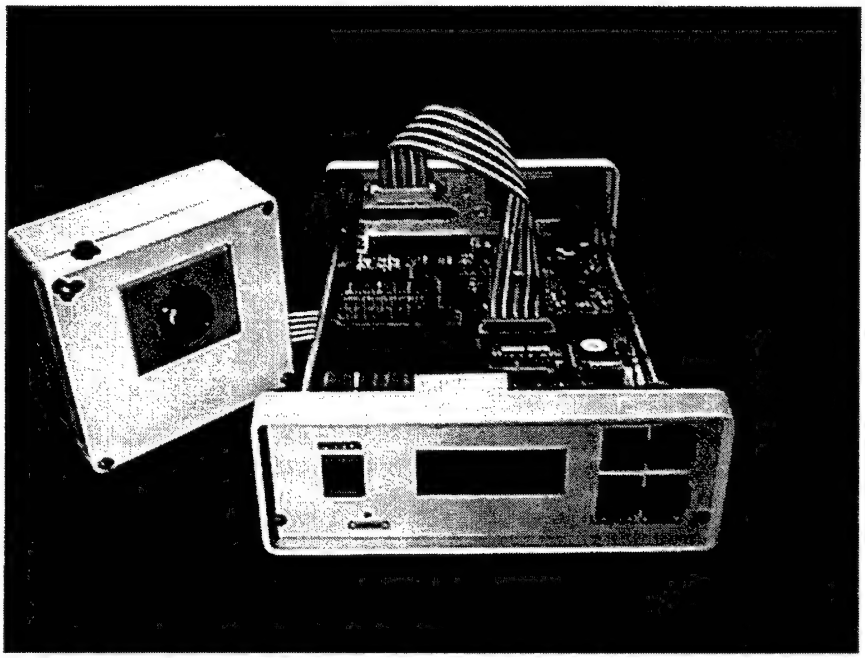


Figure 32. Demonstration camera test system.

One of the reasons stated in Section III for choosing the Σ–Δ pixel architecture for the first 3-D imager was its potential for use in more complex multi-layer systems. In order to investigate further applications for 3-D systems integration, as well as to provide a portable platform for testing the 3-D image sensor characteristics, program funds were used to build a demonstration test system with an on-board processor that could be programmed to operate directly on the bit streams acquired from the imager.

The system developed, shown in Figure 32, consisted of a separate camera head—which could be positioned as needed—and a main board containing an SRAM bank and an 8-bit ATMEL RISC microprocessor, which could be programmed through an external connector. The on-board memory was capable of holding up to 256 samples from a 256x256 pixel imager. Data were transmitted to a PC via the parallel port for storage or display. This system could be used for acquiring and decoding pixel bit streams or for simulating secondary pixel processors operating on the bit streams.

5.1.2. Phase Detection as a Fundamental Operation

Given that the pixel responds to incident light by oscillating at a frequency proportional to the signal intensity, changes in intensity translate into variations in the pixel's phase over time. Phase differences between two Σ–Δ pixel outputs can be measured by recording the state output of a phase-frequency detector, or PFD. The PFD is a three state Finite-State Machine as diagrammed in Figure 33.

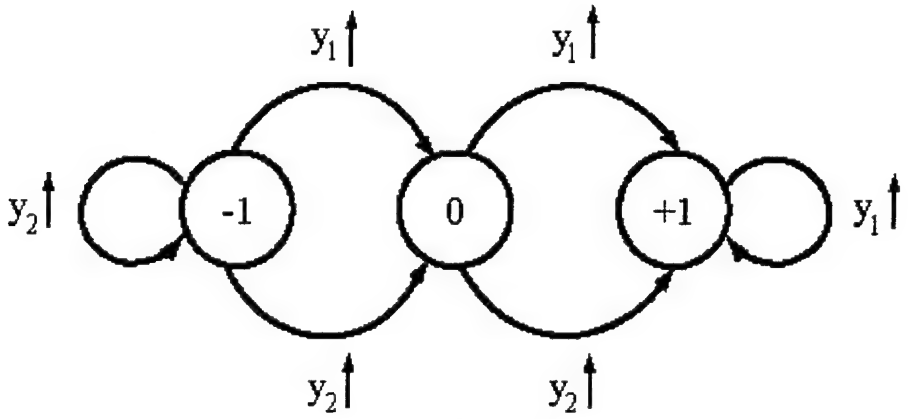


Figure 33. Phase-Frequency Detector State Diagram.

The PFD operates on two input bits streams, y_1 and y_2, and changes state when one of the streams presents a '1' and the other a '0'. If both streams present '1's there is no state change. To illustrate operation of the PFD, consider two Σ–Δ output streams y_1 and y_2 generated by inputs $x_1 = .666 f_S$ and $x_2 = .734 f_S$. Assuming no correlation between the oscillators, so that each has random initial phase, a typical pattern of bits that might be observed from each is:

y_1: 0 1 1 0 1 1 0 1 1 0 1 1 0 1 1 0 1 1 0 1
y_2: 0 1 1 0 1 1 1 0 1 1 1 0 1 1 1 0 1 1 0 1

Assuming, the PFD is initially in state 0, its output given these two inputs would be:

S: 0 0 0 0 0 0 -1 0 0 -1 -1 0 -1 -1 -1 -1 -1 -1 -1 -1

As can be seen, the state exhibits a negative trend changing from '0's to mostly '-1's over time. While this trend is indicative that $x_1 < x_2$, one can get a better idea of the phase relation between the two output streams by recording the PFD state over a longer period of time and low-pass filtering the resultant sequence. The filtered phase state over 100 samples of the above sequences is shown in Figure 34.

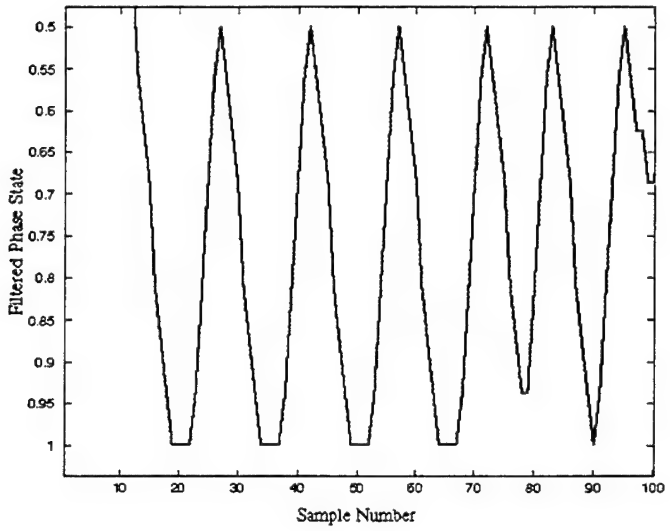


Figure 34. Filtered phase state response for Σ–Δ streams generated by x_1=.666 f_S and x_2=.734f_S.

One can observe that, after an initial transient period, the phase state stabilizes into an oscillatory pattern with a fundamental frequency equal to the difference in frequency between the two input streams. The steady-state filtered sequence is negative if $x_1 < x_2$ and positive if $x_1 > x_2$. The PFD combined with a low-pass filter can thus be used to compare two frequency signals, to generate a secondary Σ–Δ sequence driven by the difference frequency, or to provide an update signal to a voltage-controlled oscillator (VCO) to lock onto a given input signal.

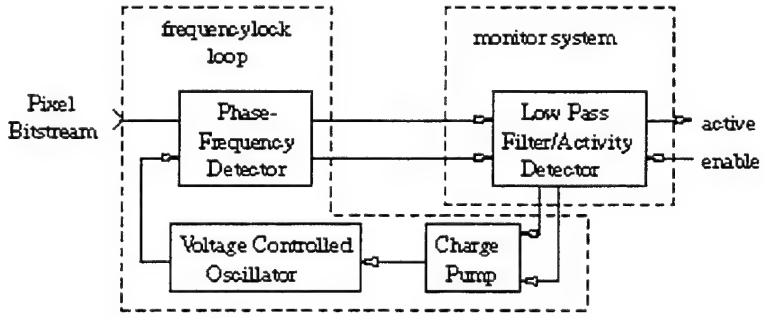


Figure 35. Phase-locked loop for data storage and tracking.

Data storage is accomplished by matching the frequency of a VCO to a Σ–Δ bit stream. Figure 35 illustrates the principle of a phase-locked loop (PLL) in which a PFD generates correction signals to a charge pump to update a VCO reference voltage via a charge pump. Once the two signals are matched, the voltage on the VCO is whatever value is required to reproduce the input frequency. Storage is achieved by breaking the feedback loop.

In addition to data storage, it is also possible to implement a variety of simple pixel-parallel algorithms with the PLL. One such algorithm is to learn activity patterns and to signal any unusual activity in a scene. This algorithm was extensively analyzed for its potential implementation as a 3-D circuit.

5.1.3. An Algorithm for Learning Activity Patterns Using Phase-Locked Loops

An activity detection system is similar to a motion tracking system, in that they both identify areas of motion in a sequence of images. While a motion tracker will assign a velocity to every pixel in the image, an activity detector assigns a scalar value to every pixel. The magnitude of this value is a measure of how "active" the system believes that pixel to be. By thresholding these values, it is possible to identify areas of the image that contain active sites. Activity detection has many potential applications. As a security device, an activity sensor would be able to monitor important areas and alert guards when something unusual has been detected. Activity detection also has the potential to reduce transmission bandwidth and storage requirements by transmitting or saving only those sections of the image where activity is occurring

A good activity detection system should have several properties. First, it should be able to differentiate between the portions of the image that are background, that is non-active, and those that are not. It should also be able to adapt to slow variations in the background. For example, as the sun moves during the course of the day, shadows shift and the incident light on the background changes. These types of variations should not trigger alerts. The ideal system should also be able to compensate for "oscillating pixels", that is pixels that alternate between two or three regular values. A tree blowing in the wind, a fluttering flag, and a traffic light are a few examples of scenes that result in oscillating pixels. These signals should also be part of the background and not affect the activity of the system.

The algorithm presented here is a modification of the multimode adaptive sensor model developed by Stauffer[19]. Using the same basic approach, a system that could be readily implemented in Silicon was developed. The key concerns in developing the modified system were to maintain a small physical footprint for the pixel processors, and to maximize modularity. A modular design would enable the system to be more economically built in 3-D Silicon, by reusing the same mask sets for different layers.

The multimode tracking system can be segmented into two components as shown in Figure 36, the pixel memory modules and the control logic. The control system is responsible for deciding which of the modules should be tasked to tracking the current input as well as deciding when the pixel input is a new value.

The main purpose of the control logic is to execute a replacement strategy for the memory modules. Specifically, during input frequency changes, it must decide which, if any, of the memory elements should be assigned to track the new signal. Two alternate strategies were examined. The first was a standard least recently used (LRU) system, and the second, a sequential approach. It was determined that the sequential replacement had the lowest cost both

in terms of area and design flexibility. The sequentially ordered replacement strategy allows for the same control logic to control an arbitrary number of memory modules. It has slightly poorer performance than the LRU strategy, but not enough to justify the extra circuitry required to implement the latter.

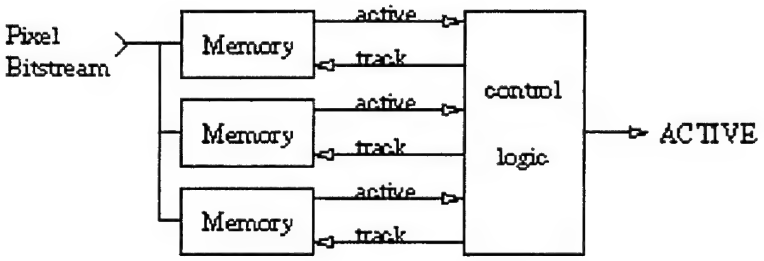


Figure 36. Multimode activity tracking system.

The memory modules are each composed of a PLL with an activity monitor placed into the feedback loop. The purpose of the monitor component is to report changes in the pixel input and decide if the charge pump should alter the VCO frequency. The monitor is placed within the loop to be able to prevent a new signal from altering the VCO frequency too quickly. The correction signal is only allowed to pass through if the module's enable signal is activated by the control logic. If the pixel input is within a specified margin of the VCO frequency, the correction signals are issued to the charge pump; otherwise a potential activity alert is passed to the control logic. The monitor is able to determine activity by estimating the fundamental frequency of the PFD output.

5.1.4. Activity Detection System Results

Using the programmable camera test system, the algorithm was implemented and tested to demonstrate how a 3-D activity detection chip might behave. In the examples shown in Figure 37, the activity detection system was tested over the course of several hours. From 6pm one evening to 10am the next morning, the simulation ran with the imager overlooking a section of the MIT AI Vision Laboratory. During that time, the simulation saved images whenever the number of active pixels exceeded a given number. Figure 37 contains the 64 images and the times at which they were taken. If the system had been configured to automatically store all of the images during the test—much like a VCR-based security camera, the data set would have contained 7,680 images and would have required 120 times more storage space. The activity detection system has distilled the data to only those frames where significant action was noted.

Images **1-A** through **1-E** are caused by the appearance of a person in the center or the image. His presence was sufficient to trigger an activity alert. The number of "active" pixels remained relatively high after the intruder left because the system had not gained a very good model for the background before the person appeared. Consequently, a few more frames of data were needed for the simulated pixel processors to relearn the background.

Figure 37. A series of images recorded over a 15-hour interval when a high level of activity was detected.

Images **1-G** through **2-H** highlight the movement of a member of the AI Lab's cleaning staff. She, like several others in the images, is very blurry due to the long integration times needed to simulate full parallelism with a serial processor. The woman can be seen most clearly in image **2-B**. Images **3-A** through **3-F** contain the faint trace of a person walking in front of the camera. Again, the motion was too rapid to allow a clear picture. At 7:58 pm, a person can be seen looking into the office. At 8:06 another figure appeared in front of the office door and remained there for two minutes. No significant activity was logged until 10:06pm. At that time, the far door was opened—note the black area in image **4-E**. In the next image, **4-F**, the light in that

office was turned on, causing a significant change in intensity. The next several images were stored while the system adapted to the new background.

No notable activity was detected for the following several hours. The images in row 7 show the return of the office occupant opening the door and leaving it ajar. Row 8 contains the blurs of people walking in front of the camera. The majority of the images capture periods of easily recognizable activity. Noticeably absent are any images corresponding to sunrise. The slowly increasing light levels were learned by the system and did not trigger any activity.

6. Conclusions and Recommendations

The work completed in this program represents a truly revolutionary advance in semiconductor processing and circuit design technology. A year after the program began, in 1997, the Semiconductor Industry Association (SIA) announced that major obstacles existed on the technology roadmap that would prevent the industry from continuing historical trends in performance improvements beyond 2005. One of these obstacles was the bottleneck presented by two-dimensional CMOS interconnect limitations. A few months after completion of the 3-D program, the team presented to a packed room at the International Solid State Circuits Convention (ISSCC) in February 2001, the world's first fully-functional 3-D image sensor with pixel-parallel A/D conversion.

3-D integration represents a next step towards achieving high density systems-on-a-chip. It has become clear during the course of this work, however, that further improvements in the technology and design environment will be necessary before 3-D integrated circuit fabrication can compete against 2D CMOS processing for density and performance. We recommend that work be continued in the following areas to make 3-D fabrication a competitive mainstream technology.

- **Via Size:** 3-D vias must be reduced in size to the dimensions of typical interlevel metal vias in 2D CMOS. In the current program, 6-μm vias could be reliably produced with a +/- 2μm surround for alignment tolerance. In future 3-D chips, vias will have to have sub-micron dimensions—typically 0.5μm cuts—with +/- 0.25μm surrounds. Achieving this goal will require techniques for filling aspect ratio via cuts with metal, and for aligning wafers to within 100nm tolerance.

- **Low Temperature Oxide Bonding:** In order to make multi-layer devices, the epoxy adhesive used here for bonding two wafers will have to be replaced with a more stable material that can withstand subsequent thermal cycles—to at least 475°C—in order to use a metal filling process for the 3-D vias and to then sinter the metal for low resistance contacts.

- **Die-level Processing:** In order to improve the yield for multi-layer, devices, it will be necessary to test for known good die and to bond only functional die on the stack. This will mean that current wafer-to-wafer processing tools will have to be adapted for die-to-wafer, or die-to-die processing.

- **CAD Tool Development:** In order to allow circuit designers to become proficient in 3-D circuit design, new design tools will be needed to allow, at a minimum, physical layout, design rule verification, and layout vs. schematic checking.

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Appendix A. Academic Theses Supported

1. C. A. Lewis, *Evaluation of the Spectral Response for Thin Epi Back-Illuminated Photodiodes*, M.S. Thesis ECE Dept., Northeastern University, May 2000.

2. V. C. Lum, *An Activity Detection System for Frequency-Encoded Pixels*, M-Eng Thesis EECS Dept., MIT, May 2000.

3. A. Kumar, *A New Topology for a Wide Linear Range, Rail-to-Rail Constant g_m Subthreshold Operational Transconductance Amplifier*, MS Thesis ECE Dept., Northeastern University, October, 1998.

Appendix B. Three-Dimensional Integrated Circuit Fabrication

The fabrication of three-dimensional stacked integrated circuits requires precise alignment of a pair of completed device wafers, followed by a bonding process that maintains close contact between the surfaces (typically 3-5 microns). In the present method, a solvent-less epoxy is used to bond the wafers, which is cured at an elevated temperature under applied pressure. The alignment of the wafer pair is maintained during the curing cycle. Once the wafers have been successfully bonded, the top wafer is etched down to its buried oxide layer (the top wafer is always SOI, at present). Vias are etched through the oxide layers and aluminum is deposited and patterned to connect the circuit layers. The fabrication process is listed below:

1. Polish the backsides of the wafers to facilitate alignment.

2. Clean the wafer surfaces in a megasonic DI rinse to remove particles and inspect for defects using a green light or Surfscan.

3. Mix, degas, and filter the bonding epoxy.

4. Insert the top wafer into the Karl Suss contact aligner face down (i.e., in place of a photomask) and apply vacuum to hold it in place. (The system is set up for infrared alignment).

5. Insert the bottom wafer into the aligner on the vacuum chuck.

6. Apply 70 μl of epoxy to the center of the bottom wafer.

7. Bring the wafers into contact and then separate them to the desired alignment gap.

8. Align the wafers using IR optics and brought them into contact. (Note: when the wafers are aligned and contacted, the epoxy spreads out from the center of the pair.)

9. Release the top wafer vacuum.

10. Bring the wafer chuck out of contact. The wafer pair is now attached to the chuck and remains in alignment.

11. Apply a fast setting epoxy to the edges of the wafer pair and cure it. This ensures that the wafers remain in alignment when they are removed from the wafer chuck.

12. Transfer the wafer pair to the bonding jig.

13. Cure the epoxy under pressure in the jig. During the cycle, an intermediate temperature (~70°C) step reduces the viscosity of the epoxy, allowing it to completely fill the space between the wafers. The temperature is then increased to fully cure the epoxy.

14. Etch the handle Silicon of the top wafer to a thickness of about 20μm in HNA using the CCD back-illumination etching apparatus.

15. Etch the remaining Silicon from the Box using TMAH.

16. Pattern the shallow vias using standard I-line lithography. The stepper jobs are written to utilize the "correct" alignment marks; that is, the top layer is flipped along the y-axis and the machine must be set up to perform the alignment.

17. Plasma etch the vias using a standard oxide etch recipe. It is critical to ensure that the wafer is kept cool during the etch to prevent degradation of the epoxy layer.

18. Remove the remaining resist in an oxygen etch.

19. Pattern the deep vias.

20. Etch the oxide in the deep vias then etch the epoxy in an oxygen plasma at -100°C to reduce undercut. This step also removes the photoresist.

21. Deposit aluminum by RF bias sputtering. The wafer is attached to a water-cooled platen to avoid heating. An in-situ sputter etch is included prior to deposition to remove oxide on the surface of the metal layers.

22. Pattern the aluminum using the backmetal mask.

23. Wet etch the backmetal in PAN etchant.

24. Strip the resist in acetone and isopropanol.

25. At this point, the circuit fabrication is complete and the devices can be tested. Additional processing is required to "flip" the circuits for backside illumination of the imager epitaxial layer.

Appendix C. Test Device Characterization

I. Transistor characteristics vs. channel length

- ***DEVICE-1***

Row2 Col1 (left)
N-channel transistor (No Well) Width = 20.0μm, Length = 20.0 μm

- TEST1 - VTLOW
- TEST2 - NO TEST - 888 CODE
- TEST3 - VTHIGH
- TEST4 - CALCULATE DIBL
- TEST5 - SUBTHRESHOLD SLOPE
- TEST6 - DRAIN-SOURCE LEAKAGE W/ 2.5V ON DRAIN, 0V ON GATE
- TEST7 - DRAIN-SOURCE LEAKAGE W/ 5.0V ON DRAIN, 0V ON GATE
- TEST8 - DRAIN-SOURCE LEAKAGE W/ 5.0V ON DRAIN, -.5V ON GATE
- TEST9 - DRIVE CURRENT W/ GATE AND DRAIN @ 2.5V
- TEST10 - DRIVE CURRENT W/ GATE AND DRAIN @ 5.0V
- TEST11 - LINEAR TRANSCONDUCTANCE (GM)
- TEST12 - TRANSCONDUCTANCE IN SATURATION (GSAT)
- TEST13 - OUTPUT CONDUCTANCE (GDS)
- TEST14 - NO TEST - 888 CODE

- ***DEVICE-2***

Row2 Col1 (right)
N-channel transistor (No Well) Width = 20.0μm, Length = 2.0 μm

- TEST15 - VTLOW
- TEST16 - NO TEST - 888 CODE
- TEST17 - VTHIGH
- TEST18 - CALCULATE DIBL
- TEST19 - SUBTHRESHOLD SLOPE
- TEST20 - DRAIN-SOURCE LEAKAGE W/ 2.5V ON DRAIN, 0V ON GATE
- TEST21 - DRAIN-SOURCE LEAKAGE W/ 5.0V ON DRAIN, 0V ON GATE
- TEST22 - DRAIN-SOURCE LEAKAGE W/ 5.0V ON DRAIN, -.5V ON GATE
- TEST23 - DRIVE CURRENT W/ GATE AND DRAIN @ 2.5V
- TEST24 - DRIVE CURRENT W/ GATE AND DRAIN @ 5.0V
- TEST25 - LINEAR TRANSCONDUCTANCE (GM)
- TEST26 - TRANSCONDUCTANCE IN SATURATION (GSAT)
- TEST27 - OUTPUT CONDUCTANCE (GDS)
- TEST28 - NO TEST - 888 CODE

- ***DEVICE-3***

Row2 Col2 (left)
N-channel transistor (No Well) Width = 20.0μm, Length = 0.8 μm

- TEST29 - VTLOW
- TEST30 - NO TEST - 888 CODE
- TEST31 - VTHIGH
- TEST32 - CALCULATE DIBL
- TEST33 - SUBTHRESHOLD SLOPE
- TEST34 - DRAIN-SOURCE LEAKAGE W/ 2.5V ON DRAIN, 0V ON GATE
- TEST35 - DRAIN-SOURCE LEAKAGE W/ 5.0V ON DRAIN, 0V ON GATE
- TEST36 - DRAIN-SOURCE LEAKAGE W/ 5.0V ON DRAIN, -.5V ON GATE
- TEST37 - DRIVE CURRENT W/ GATE AND DRAIN @ 2.5V
- TEST38 - DRIVE CURRENT W/ GATE AND DRAIN @ 5.0V
- TEST39 - LINEAR TRANSCONDUCTANCE (GM)
- TEST40 - TRANSCONDUCTANCE IN SATURATION (GSAT)
- TEST41 - OUTPUT CONDUCTANCE (GDS)
- TEST42 - NO TEST - 888 CODE

- ***DEVICE-4***

Row3 Col1 (left)
N-channel transistor (No Well) Width = 20.0μm, Length = 0.6 μm

- TEST43 - VTLOW
- TEST44 - NO TEST - 888 CODE
- TEST45 - VTHIGH
- TEST46 - CALCULATE DIBL
- TEST47 - SUBTHRESHOLD SLOPE
- TEST48 - DRAIN-SOURCE LEAKAGE W/ 2.5V ON DRAIN, 0V ON GATE
- TEST49 - DRAIN-SOURCE LEAKAGE W/ 5.0V ON DRAIN, 0V ON GATE
- TEST50 - DRAIN-SOURCE LEAKAGE W/ 5.0V ON DRAIN, -.5V ON GATE
- TEST51 - DRIVE CURRENT W/ GATE AND DRAIN @ 2.5V
- TEST52 - DRIVE CURRENT W/ GATE AND DRAIN @ 5.0V
- TEST53 - LINEAR TRANSCONDUCTANCE (GM)
- TEST54 - TRANSCONDUCTANCE IN SATURATION (GSAT)
- TEST55 - OUTPUT CONDUCTANCE (GDS)
- TEST56 - NO TEST - 888 CODE

- ***DEVICE-5***

Row2 Col2 (right)
N-channel transistor (P Well) Width = 20.0μm, Length = 20.0 μm

- TEST57 - VTLOW
- TEST58 - NO TEST - 888 CODE
- TEST59 - VTHIGH
- TEST60 - CALCULATE DIBL
- TEST61 - SUBTHRESHOLD SLOPE
- TEST62 - DRAIN-SOURCE LEAKAGE W/ 2.5V ON DRAIN, 0V ON GATE
- TEST63 - DRAIN-SOURCE LEAKAGE W/ 5.0V ON DRAIN, 0V ON GATE
- TEST64 - DRAIN-SOURCE LEAKAGE W/ 5.0V ON DRAIN, -.5V ON GATE
- TEST65 - DRIVE CURRENT W/ GATE AND DRAIN @ 2.5V
- TEST66 - DRIVE CURRENT W/ GATE AND DRAIN @ 5.0V
- TEST67 - LINEAR TRANSCONDUCTANCE (GM)
- TEST68 - TRANSCONDUCTANCE IN SATURATION (GSAT)
- TEST69 - OUTPUT CONDUCTANCE (GDS)
- TEST70 - NO TEST - 888 CODE

- ***DEVICE-6***

Row2 Col3 (left)
N-channel transistor (P Well) Width = 20.0μm, Length = 2.0 μm

- TEST71 - VTLOW
- TEST72 - NO TEST - 888 CODE
- TEST73 - VTHIGH
- TEST74 - CALCULATE DIBL
- TEST75 - SUBTHRESHOLD SLOPE
- TEST76 - DRAIN-SOURCE LEAKAGE W/ 2.5V ON DRAIN, 0V ON GATE
- TEST77 - DRAIN-SOURCE LEAKAGE W/ 5.0V ON DRAIN, 0V ON GATE
- TEST78 - DRAIN-SOURCE LEAKAGE W/ 5.0V ON DRAIN, -.5V ON GATE
- TEST79 - DRIVE CURRENT W/ GATE AND DRAIN @ 2.5V
- TEST80 - DRIVE CURRENT W/ GATE AND DRAIN @ 5.0V
- TEST81 - LINEAR TRANSCONDUCTANCE (GM)
- TEST82 - TRANSCONDUCTANCE IN SATURATION (GSAT)
- TEST83 - OUTPUT CONDUCTANCE (GDS)
- TEST84 - NO TEST - 888 CODE

- ***DEVICE-7***

Row2 Col3 (right)
N-channel transistor (P Well) Width = 20.0μm, Length = .8 μm

- TEST85 - VTLOW
- TEST86 - NO TEST - 888 CODE

- TEST87 - VTHIGH
- TEST88 - CALCULATE DIBL
- TEST89 - SUBTHRESHOLD SLOPE
- TEST90 - DRAIN-SOURCE LEAKAGE W/ 2.5V ON DRAIN, 0V ON GATE
- TEST91 - DRAIN-SOURCE LEAKAGE W/ 5.0V ON DRAIN, 0V ON GATE
- TEST92 - DRAIN-SOURCE LEAKAGE W/ 5.0V ON DRAIN, -.5V ON GATE
- TEST93 - DRIVE CURRENT W/ GATE AND DRAIN @ 2.5V
- TEST94 - DRIVE CURRENT W/ GATE AND DRAIN @ 5.0V
- TEST95 - LINEAR TRANSCONDUCTANCE (GM)
- TEST96 - TRANSCONDUCTANCE IN SATURATION (GSAT)
- TEST97 - OUTPUT CONDUCTANCE (GDS)
- TEST98 - NO TEST - 888 CODE

- ***DEVICE-8***

Row3 Col2 (right)
N-channel transistor (P Well) Width = 20.0μm, Length = 0.6 μm

- TEST99 - VTLOW
- TEST100 - NO TEST - 888 CODE
- TEST101 - VTHIGH
- TEST102 - CALCULATE DIBL
- TEST103 - SUBTHRESHOLD SLOPE
- TEST104 - DRAIN-SOURCE LEAKAGE W/ 2.5V ON DRAIN, 0V ON GATE
- TEST105 - DRAIN-SOURCE LEAKAGE W/ 5.0V ON DRAIN, 0V ON GATE
- TEST106 - DRAIN-SOURCE LEAKAGE W/ 5.0V ON DRAIN, -.5V ON GATE
- TEST107 - DRIVE CURRENT W/ GATE AND DRAIN @ 2.5V
- TEST108 - DRIVE CURRENT W/ GATE AND DRAIN @ 5.0V
- TEST109 - LINEAR TRANSCONDUCTANCE (GM)
- TEST110 - TRANSCONDUCTANCE IN SATURATION (GSAT)
- TEST111 - OUTPUT CONDUCTANCE (GDS)
- TEST112 - NO TEST - 888 CODE

- ***DEVICE-9***

Row2 Col4 (left)
N-channel transistor (Nch Depletion in Pwell) Width = 20.0μm, Length = 20.0 μm

- TEST113 - VTLOW
- TEST114 - NO TEST - 888 CODE
- TEST115 - VTHIGH
- TEST116 - CALCULATE DIBL
- TEST117 - SUBTHRESHOLD SLOPE

- TEST118 - DRAIN-SOURCE LEAKAGE W/ -2.5V ON DRAIN, 0V ON GATE
- TEST119 - DRAIN-SOURCE LEAKAGE W/ -5.0V ON DRAIN, 0V ON GATE
- TEST120 - DRAIN-SOURCE LEAKAGE W/ -5.0V ON DRAIN, .5V ON GATE
- TEST121 - DRIVE CURRENT W/ GATE AND DRAIN @ -2.5V
- TEST122 - DRIVE CURRENT W/ GATE AND DRAIN @ -5.0V
- TEST123 - LINEAR TRANSCONDUCTANCE (GM)
- TEST124 - TRANSCONDUCTANCE IN SATURATION (GSAT)
- TEST125 - OUTPUT CONDUCTANCE (GDS)
- TEST126 - NO TEST - 888 CODE

- ***DEVICE-10***

Row2 Col4 (right)
N-channel transistor (Nch Depletion in Pwell) Width = 20.0μm, Length = 2.0 μm

- TEST127 - VTLOW
- TEST128 - NO TEST - 888 CODE
- TEST129 - VTHIGH
- TEST130 - CALCULATE DIBL
- TEST131 - SUBTHRESHOLD SLOPE
- TEST132 - DRAIN-SOURCE LEAKAGE W/ -2.5V ON DRAIN, 0V ON GATE
- TEST133 - DRAIN-SOURCE LEAKAGE W/ -5.0V ON DRAIN, 0V ON GATE
- TEST134 - DRAIN-SOURCE LEAKAGE W/ -5.0V ON DRAIN, .5V ON GATE
- TEST135 - DRIVE CURRENT W/ GATE AND DRAIN @ -2.5V
- TEST136 - DRIVE CURRENT W/ GATE AND DRAIN @ -5.0V
- TEST137 - LINEAR TRANSCONDUCTANCE (GM)
- TEST138 - TRANSCONDUCTANCE IN SATURATION (GSAT)
- TEST139 - OUTPUT CONDUCTANCE (GDS)
- TEST140 - NO TEST - 888 CODE

- ***DEVICE-11***

Row2 Col5 (left)
N-channel transistor (Nch Depletion in Pwell) Width = 20.0μm, Length = 0.8 μm

- TEST141 - VTLOW
- TEST142 - NO TEST - 888 CODE
- TEST143 - VTHIGH
- TEST144 - CALCULATE DIBL
- TEST145 - SUBTHRESHOLD SLOPE
- TEST146 - DRAIN-SOURCE LEAKAGE W/ -2.5V ON DRAIN, 0V ON GATE
- TEST147 - DRAIN-SOURCE LEAKAGE W/ -5.0V ON DRAIN, 0V ON GATE
- TEST148 - DRAIN-SOURCE LEAKAGE W/ -5.0V ON DRAIN, .5V ON GATE

- TEST149 - DRIVE CURRENT W/ GATE AND DRAIN @ -2.5V
- TEST150 - DRIVE CURRENT W/ GATE AND DRAIN @ -5.0V
- TEST151 - LINEAR TRANSCONDUCTANCE (GM)
- TEST152 - TRANSCONDUCTANCE IN SATURATION (GSAT)
- TEST153 - OUTPUT CONDUCTANCE (GDS)
- TEST154 - NO TEST - 888 CODE

- ***DEVICE-12***

Row3 Col4 (left)
N-channel transistor (Nch Depletion in Pwell) Width = 20.0μm, Length = 0.6 μm

- TEST155 - VTLOW
- TEST156 - NO TEST - 888 CODE
- TEST157 - VTHIGH
- TEST158 - CALCULATE DIBL
- TEST159 - SUBTHRESHOLD SLOPE
- TEST160 - DRAIN-SOURCE LEAKAGE W/ -2.5V ON DRAIN, 0V ON GATE
- TEST161 - DRAIN-SOURCE LEAKAGE W/ -5.0V ON DRAIN, 0V ON GATE
- TEST162 - DRAIN-SOURCE LEAKAGE W/ -5.0V ON DRAIN, .5V ON GATE
- TEST163 - DRIVE CURRENT W/ GATE AND DRAIN @ -2.5V
- TEST164 - DRIVE CURRENT W/ GATE AND DRAIN @ -5.0V
- TEST165 - LINEAR TRANSCONDUCTANCE (GM)
- TEST166 - TRANSCONDUCTANCE IN SATURATION (GSAT)
- TEST167 - OUTPUT CONDUCTANCE (GDS)
- TEST168 - NO TEST - 888 CODE

- ***DEVICE-13***

Row2 Col5 (right)
P-channel transistor Width = 20.0μm, Length = 20.0 μm

- TEST169 - VTLOW
- TEST170 - NO TEST - 888 CODE
- TEST171 - VTHIGH
- TEST172 - CALCULATE DIBL
- TEST173 - SUBTHRESHOLD SLOPE
- TEST174 - DRAIN-SOURCE LEAKAGE W/ -2.5V ON DRAIN, 0V ON GATE
- TEST175 - DRAIN-SOURCE LEAKAGE W/ -5.0V ON DRAIN, 0V ON GATE
- TEST176 - DRAIN-SOURCE LEAKAGE W/ -5.0V ON DRAIN, .5V ON GATE
- TEST177 - DRIVE CURRENT W/ GATE AND DRAIN @ -2.5V
- TEST178 - DRIVE CURRENT W/ GATE AND DRAIN @ -5.0V
- TEST179 - LINEAR TRANSCONDUCTANCE (GM)

- TEST180 - TRANSCONDUCTANCE IN SATURATION (GSAT)
- TEST181 - OUTPUT CONDUCTANCE (GDS)
- TEST182 - NO TEST - 888 CODE

- ***DEVICE-14***

Row2 Col6 (left)
P-channel transistor Width = 20.0μm, Length = 2.0 μm

- TEST183 - VTLOW
- TEST184 - NO TEST - 888 CODE
- TEST185 - VTHIGH
- TEST186 - CALCULATE DIBL
- TEST187 - SUBTHRESHOLD SLOPE
- TEST188 - DRAIN-SOURCE LEAKAGE W/ -2.5V ON DRAIN, 0V ON GATE
- TEST189 - DRAIN-SOURCE LEAKAGE W/ -5.0V ON DRAIN, 0V ON GATE
- TEST190 - DRAIN-SOURCE LEAKAGE W/ -5.0V ON DRAIN, .5V ON GATE
- TEST191 - DRIVE CURRENT W/ GATE AND DRAIN @ -2.5V
- TEST192 - DRIVE CURRENT W/ GATE AND DRAIN @ -5.0V
- TEST193 - LINEAR TRANSCONDUCTANCE (GM)
- TEST194 - TRANSCONDUCTANCE IN SATURATION (GSAT)
- TEST195 - OUTPUT CONDUCTANCE (GDS)
- TEST196 - NO TEST - 888 CODE

- ***DEVICE-15***

Row2 Col6 (right)
P-channel transistor Width = 20.0μm, Length = 0.8 μm

- TEST197 - VTLOW
- TEST198 - NO TEST - 888 CODE
- TEST199 - VTHIGH
- TEST200 - CALCULATE DIBL
- TEST201 - SUBTHRESHOLD SLOPE
- TEST202 - DRAIN-SOURCE LEAKAGE W/ -2.5V ON DRAIN, 0V ON GATE
- TEST203 - DRAIN-SOURCE LEAKAGE W/ -5.0V ON DRAIN, 0V ON GATE
- TEST204 - DRAIN-SOURCE LEAKAGE W/ -5.0V ON DRAIN, .5V ON GATE
- TEST205 - DRIVE CURRENT W/ GATE AND DRAIN @ -2.5V
- TEST206 - DRIVE CURRENT W/ GATE AND DRAIN @ -5.0V
- TEST207 - LINEAR TRANSCONDUCTANCE (GM)
- TEST208 - TRANSCONDUCTANCE IN SATURATION (GSAT)
- TEST209 - OUTPUT CONDUCTANCE (GDS)
- TEST210 - NO TEST - 888 CODE

- ***DEVICE-16***

Row3 Col5 (right)
P-channel transistor Width = 20.0μm, Length = 0.6 μm

- TEST211 - VTLOW
- TEST212 - NO TEST - 888 CODE
- TEST213 - VTHIGH
- TEST214 - CALCULATE DIBL
- TEST215 - SUBTHRESHOLD SLOPE
- TEST216 - DRAIN-SOURCE LEAKAGE W/ -2.5V ON DRAIN, 0V ON GATE
- TEST217 - DRAIN-SOURCE LEAKAGE W/ -5.0V ON DRAIN, 0V ON GATE
- TEST218 - DRAIN-SOURCE LEAKAGE W/ -5.0V ON DRAIN, .5V ON GATE
- TEST219 - DRIVE CURRENT W/ GATE AND DRAIN @ -2.5V
- TEST220 - DRIVE CURRENT W/ GATE AND DRAIN @ -5.0V
- TEST221 - LINEAR TRANSCONDUCTANCE (GM)
- TEST222 - TRANSCONDUCTANCE IN SATURATION (GSAT)
- TEST223 - OUTPUT CONDUCTANCE (GDS)
- TEST224 - NO TEST - 888 CODE

II. Transistor characteristics vs. channel width

- ***DEVICE-17***

Row4 Col1 (left)
N-channel transistor (No Well) Width = 2.0 μm, Length = 0.8 μm

- TEST225 - VTLOW
- TEST226 - NO TEST - 888 CODE
- TEST227 - VTHIGH
- TEST228 - CALCULATE DIBL
- TEST229 - SUBTHRESHOLD SLOPE
- TEST230 - DRAIN-SOURCE LEAKAGE W/ 2.5V ON DRAIN, 0V ON GATE
- TEST231 - DRAIN-SOURCE LEAKAGE W/ 5.0V ON DRAIN, 0V ON GATE
- TEST232 - DRAIN-SOURCE LEAKAGE W/ 5.0V ON DRAIN, -.5V ON GATE
- TEST233 - DRIVE CURRENT W/ GATE AND DRAIN @ 2.5V
- TEST234 - DRIVE CURRENT W/ GATE AND DRAIN @ 5.0V
- TEST235 - LINEAR TRANSCONDUCTANCE (GM)
- TEST236 - TRANSCONDUCTANCE IN SATURATION (GSAT)
- TEST237 - OUTPUT CONDUCTANCE (GDS)
- TEST238 - NO TEST - 888 CODE

- ***DEVICE-18***

Row5 Col1 (right)
N-channel transistor (No Well) Width = 0.8μm, Length = 0.8 μm

- TEST239 - VTLOW
- TEST240 - NO TEST - 888 CODE
- TEST241 - VTHIGH
- TEST242 - CALCULATE DIBL
- TEST243 - SUBTHRESHOLD SLOPE
- TEST244 - DRAIN-SOURCE LEAKAGE W/ 2.5V ON DRAIN, 0V ON GATE
- TEST245 - DRAIN-SOURCE LEAKAGE W/ 5.0V ON DRAIN, 0V ON GATE
- TEST246 - DRAIN-SOURCE LEAKAGE W/ 5.0V ON DRAIN, -.5V ON GATE
- TEST247 - DRIVE CURRENT W/ GATE AND DRAIN @ 2.5V
- TEST248 - DRIVE CURRENT W/ GATE AND DRAIN @ 5.0V
- TEST249 - LINEAR TRANSCONDUCTANCE (GM)
- TEST250 - TRANSCONDUCTANCE IN SATURATION (GSAT)
- TEST251 - OUTPUT CONDUCTANCE (GDS)
- TEST252 - NO TEST - 888 CODE

- ***DEVICE-19***

Row4 Col2 (right)
N-channel transistor (P Well) Width = 2.0μm, Length = 0.8 μm

- TEST253 - VTLOW
- TEST254 - NO TEST - 888 CODE
- TEST255 - VTHIGH
- TEST256 - CALCULATE DIBL
- TEST257 - SUBTHRESHOLD SLOPE
- TEST258 - DRAIN-SOURCE LEAKAGE W/ 2.5V ON DRAIN, 0V ON GATE
- TEST259 - DRAIN-SOURCE LEAKAGE W/ 5.0V ON DRAIN, 0V ON GATE
- TEST260 - DRAIN-SOURCE LEAKAGE W/ 5.0V ON DRAIN, -.5V ON GATE
- TEST261 - DRIVE CURRENT W/ GATE AND DRAIN @ 2.5V
- TEST262 - DRIVE CURRENT W/ GATE AND DRAIN @ 5.0V
- TEST263 - LINEAR TRANSCONDUCTANCE (GM)
- TEST264 - TRANSCONDUCTANCE IN SATURATION (GSAT)
- TEST265 - OUTPUT CONDUCTANCE (GDS)
- TEST266 - NO TEST - 888 CODE

- ***DEVICE-20***

Row5 Col3 (left)

N-channel transistor (P Well) Width = 0.8 μm, Length = 0.8 μm

- TEST267 - VTLOW
- TEST268 - NO TEST - 888 CODE
- TEST269 - VTHIGH
- TEST270 - CALCULATE DIBL
- TEST271 - SUBTHRESHOLD SLOPE
- TEST272 - DRAIN-SOURCE LEAKAGE W/ 2.5V ON DRAIN, 0V ON GATE
- TEST273 - DRAIN-SOURCE LEAKAGE W/ 5.0V ON DRAIN, 0V ON GATE
- TEST274 - DRAIN-SOURCE LEAKAGE W/ 5.0V ON DRAIN, -.5V ON GATE
- TEST275 - DRIVE CURRENT W/ GATE AND DRAIN @ 2.5V
- TEST276 - DRIVE CURRENT W/ GATE AND DRAIN @ 5.0V
- TEST277 - LINEAR TRANSCONDUCTANCE (GM)
- TEST278 - TRANSCONDUCTANCE IN SATURATION (GSAT)
- TEST279 - OUTPUT CONDUCTANCE (GDS)
- TEST280 - NO TEST - 888 CODE

- ***DEVICE-21***

Row4 Col4 (left)
N-channel transistor (Nch Depletion in Pwell) Width = 2.0μm, Length = 0.8 μm

- TEST281 - VTLOW
- TEST282 - NO TEST - 888 CODE
- TEST283 - VTHIGH
- TEST284 - CALCULATE DIBL
- TEST285 - SUBTHRESHOLD SLOPE
- TEST286 - DRAIN-SOURCE LEAKAGE W/ -2.5V ON DRAIN, 0V ON GATE
- TEST287 - DRAIN-SOURCE LEAKAGE W/ -5.0V ON DRAIN, 0V ON GATE
- TEST288 - DRAIN-SOURCE LEAKAGE W/ -5.0V ON DRAIN, .5V ON GATE
- TEST289 - DRIVE CURRENT W/ GATE AND DRAIN @ -2.5V
- TEST290 - DRIVE CURRENT W/ GATE AND DRAIN @ -5.0V
- TEST291 - LINEAR TRANSCONDUCTANCE (GM)
- TEST292 - TRANSCONDUCTANCE IN SATURATION (GSAT)
- TEST293 - OUTPUT CONDUCTANCE (GDS)
- TEST294 - NO TEST - 888 CODE

- ***DEVICE-22***

Row5 Col4 (right)
N-channel transistor (Nch Depletion in Pwell) Width = 0.8 μm, Length = 0.8 μm

- TEST295 - VTLOW
- TEST296 - NO TEST - 888 CODE
- TEST297 - VTHIGH
- TEST298 - CALCULATE DIBL
- TEST299 - SUBTHRESHOLD SLOPE
- TEST300 - DRAIN-SOURCE LEAKAGE W/ -2.5V ON DRAIN, 0V ON GATE
- TEST301 - DRAIN-SOURCE LEAKAGE W/ -5.0V ON DRAIN, 0V ON GATE
- TEST302 - DRAIN-SOURCE LEAKAGE W/ -5.0V ON DRAIN, .5V ON GATE
- TEST303 - DRIVE CURRENT W/ GATE AND DRAIN @ -2.5V
- TEST304 - DRIVE CURRENT W/ GATE AND DRAIN @ -5.0V
- TEST305 - LINEAR TRANSCONDUCTANCE (GM)
- TEST306 - TRANSCONDUCTANCE IN SATURATION (GSAT)
- TEST307 - OUTPUT CONDUCTANCE (GDS)
- TEST308 - NO TEST - 888 CODE

- ***DEVICE-23***

Row4 Col5 (right)
P-channel transistor Width = 2.0μm, Length = 0.8 μm

- TEST309 - VTLOW
- TEST310 - NO TEST - 888 CODE
- TEST311 - VTHIGH
- TEST312 - CALCULATE DIBL
- TEST313 - SUBTHRESHOLD SLOPE
- TEST314 - DRAIN-SOURCE LEAKAGE W/ -2.5V ON DRAIN, 0V ON GATE
- TEST315 - DRAIN-SOURCE LEAKAGE W/ -5.0V ON DRAIN, 0V ON GATE
- TEST316 - DRAIN-SOURCE LEAKAGE W/ -5.0V ON DRAIN, .5V ON GATE
- TEST317 - DRIVE CURRENT W/ GATE AND DRAIN @ -2.5V
- TEST318 - DRIVE CURRENT W/ GATE AND DRAIN @ -5.0V
- TEST319 - LINEAR TRANSCONDUCTANCE (GM)
- TEST320 - TRANSCONDUCTANCE IN SATURATION (GSAT)
- TEST321 - OUTPUT CONDUCTANCE (GDS)
- TEST322 - NO TEST - 888 CODE

- ***DEVICE-24***

Row5 Col6 (left)
P-channel transistor Width = 0.8 μm, Length = 0.8 μm

- TEST323 - VTLOW
- TEST324 - NO TEST - 888 CODE
- TEST325 - VTHIGH

- TEST326 - CALCULATE DIBL
- TEST327 - SUBTHRESHOLD SLOPE
- TEST328 - DRAIN-SOURCE LEAKAGE W/ -2.5V ON DRAIN, 0V ON GATE
- TEST329 - DRAIN-SOURCE LEAKAGE W/ -5.0V ON DRAIN, 0V ON GATE
- TEST400 - DRAIN-SOURCE LEAKAGE W/ -5.0V ON DRAIN, .5V ON GATE
- TEST401 - DRIVE CURRENT W/ GATE AND DRAIN @ -2.5V
- TEST402 - DRIVE CURRENT W/ GATE AND DRAIN @ -5.0V
- TEST403 - LINEAR TRANSCONDUCTANCE (GM)
- TEST404 - TRANSCONDUCTANCE IN SATURATION (GSAT)
- TEST405 - OUTPUT CONDUCTANCE (GDS)
- TEST406 - NO TEST - 888 CODE

III. ISOLATION TRANSISTORS

- ***DEVICE-25***

Row1 Col7 (right)
N-channel ISO Length = 4.0 μm

- TEST407 - DRAIN-SOURCE LEAKAGE W/ 5.0V ON DRAIN, 5.0V ON GATE

- ***DEVICE-26***

Row2 Col7 (right)
N-channel ISO Length = 2.0 μm

- TEST408 - DRAIN-SOURCE LEAKAGE W/ 5.0V ON DRAIN, 5.0V ON GATE

- ***DEVICE-27***

Row1 Col8 (right)
P-channel ISO Length = 4.0 μm

- TEST409 - DRAIN-SOURCE LEAKAGE W/ -5.0V ON DRAIN, -5.0V ON GATE

- ***DEVICE-28***

Row2 Col8 (right)
N-channel ISO Length = 2.0 μm

- TEST410 - DRAIN-SOURCE LEAKAGE W/ -5.0V ON DRAIN, -5.00V ON GATE

IV. INVERTER TEST

- ***DEVICE-29***

Row1 Col9
Inverter

For TEST411 and TEST412...

VIMS1 applies 5.0V to VDD with a 10ma limit. Vss is connected to ground. The INPUT and OUTPUT pads are connected together. The voltage on the I/O pads is measured as VINV. The I/O pads are unshorted. Current from VIMS1 is now measured with the INPUT pad set at VINV volts by VIMS2. The current is IINV.

- TEST411 - VINV
- TEST412 - IINV

For TEST413 and TEST414...

The VDD voltage from VIMS1 is reduced to 0.0V. VIMS2 applies 5.0V on the INPUT pad. VIMS3 is set up as a voltmeter and is connected to the OUTPUT pad. VDD is ramped up to 5V at 1V/ms. The voltage on the OUTPUT pad is then measured as VLOW. VIMS2 voltage is reduced to 0.0 V and the OUTPUT pad is then measured as VHIGH.

- TEST413 - VLOW
- TEST414 - VHIGH

For TEST415

(GAIN MEASUREMENT)- VAL = VINV - 30mV and VAH = VINV + 30mV. The VIMS is set to apply VAL to the INPUT pad. The OUTPUT pad voltage is measured as VOL. The INPUT pad voltage is measured as VIL. The VIMS now applies VAH to the INPUT pad. The INPUT pad voltage is measured as VIH and the OUTPUT pad voltage is measured as VOH. The Gain = (VOH-VOL)/(VIH-VIL).

- TEST415 - INVERTER GAIN MEASUREMENT

V. FIELD THRESHOLD TRANSISTORS

- ***DEVICE-30***

Row3 Col10(left)
P-channel Poly FT Width = 20.0 μm, Length = 3.0 μm

- TEST416 - -5.0V - Drain, Ground - Source, Binary Search on Gate 0V - -12V trigger on Ids = 20nA

- ***DEVICE-31***

Row5 Col10(left)
P-channel Metal FT Width = 20.0 μm, Length = 3.0 μm

- TEST417 - -5.0V - Drain, Ground - Source, Binary Search on Gate 0V - -20V trigger on Ids = 20nA

- ***DEVICE-32***

Row3 Col11(left)
N-channel Poly FT Width = 20.0 μm, Length = 3.0 μm

- TEST418 - +5.0V - Drain, Ground - Source, Binary Search on Gate 0V - 12V trigger on Ids = 20nA

- ***DEVICE-33***

Row5 Col11(left)
N-channel Metal FT Width = 20.0 μm, Length = 3.0 μm

- TEST419 - +5.0V - Drain, Ground - Source, Binary Search on Gate 0V - 20V trigger on Ids = 20nA

VI. SHEET RHO, CONTACT RESISTANCE, VIA CHAINS DELTA LINE WIDTH MEASUREMENTS

- ***DEVICE-34***

Row1 Col13
N+ Sheet Rho, Contact Resistance and Delta Line Width Device (in Pwell)

- TEST420 - N+ SHEET RESISTANCE
- TEST421 - METAL1/N+ CONTACT RESISTANCE
- TEST422 - N+ DELTAW

- ***DEVICE-35***

Row1 Col14
P+ Sheet Rho, Contact Resistance and Delta Line Width Device (in Nwell)

- TEST423 - P+ SHEET RESISTANCE
- TEST424 - METAL1/P+ CONTACT RESISTANCE
- TEST425 - P+ DELTAW

- ***DEVICE-36***

Row2 Col13
Poly Sheet Rho, Contact Resistance and Delta Line Width Device

- TEST426 - Poly SHEET RESISTANCE
- TEST427 - METAL1/Poly CONTACT RESISTANCE
- TEST428 - Poly DELTAW

- ***DEVICE-37***

Row2 Col14
Metal1 Sheet Rho, Contact Resistance and Delta Line Width Device

- TEST429 - METAL1 SHEET RESISTANCE
- TEST430 - METAL1/METAL2 CONTACT RESISTANCE
- TEST431 - METAL1 DELTAW

- ***DEVICE-38***

Row3 Col13
Depletion Sheet Rho, Contact Resistance and Delta Line Width Device (in Pwell)

- TEST432 - Depletion SHEET RESISTANCE
- TEST433 - METAL1/Depletion CONTACT RESISTANCE
- TEST434 - Depletion DELTAW

- ***DEVICE-39***

Row3 Col14
Metal2 Sheet Rho, Contact Resistance and Delta Line Width Device

- TEST435 - METAL2 SHEET RESISTANCE
- TEST436 - METAL1/METAL2 CONTACT RESISTANCE
- TEST437 - METAL2 DELTAW

- ***DEVICE-40***

Row4 Col14

Sheet Rho

- TEST438 - NWELL SURROUNDED BY PWELL SHEET RESISTANCE
- TEST439 - NWELL SHEET RESISTANCE

- ***DEVICE-41***

Row3 Col16

Top = Poly Serpentine thru Poly Comb and Island Ladder

- TEST440 - POLY SNAKE CONTINUITY
- TEST441 - POLY SNAKE TO POLY COMB LEAKAGE @ 50mV
- TEST442 - POLY SNAKE TO POLY COMB LEAKAGE @ 5.0V
- TEST443 - POLY SNAKE/COMB TO ISLAND LADDER LEAKAGE @ 50mV
- TEST444 - POLY SNAKE/COMB TO ISLAND LADDER LEAKAGE @ 5.0V

Bottom = Metal2 Serpentine thru Metal2 Comb and Metal1 Ladder

- TEST445 - METAL2 SNAKE CONTINUITY
- TEST446 - METAL2 SNAKE TO METAL2 COMB LEAKAGE @ 50mV
- TEST447 - METAL2 SNAKE TO METAL2 COMB LEAKAGE @ 5.0V
- TEST448 - METAL2 SNAKE/COMB TO METAL1 LADDER LEAKAGE @ 50mV
- TEST449 - METAL2 SNAKE/COMB TO METAL1 LADDER LEAKAGE @ 5.0V

- ***DEVICE-42***

Row3 Col17

Top = Metal1 Serpentine thru Metal1 Comb and Poly Ladder

- TEST450 - METAL1 SNAKE CONTINUITY
- TEST451 - METAL1 SNAKE TO METAL1 COMB LEAKAGE @ 50mV
- TEST452 - METAL1 SNAKE TO METAL1 COMB LEAKAGE @ 5.0V
- TEST453 - METAL1 SNAKE/COMB TO POLY LADDER LEAKAGE @ 50mV
- TEST454 - METAL1 SNAKE/COMB TO POLY LADDER LEAKAGE @ 5.0V

- ***DEVICE-43***

Row1$^{1/2}$ Col21

Top = Poly Serpentine thru Poly Comb and Island Ladder

- TEST455 - POLY SNAKE CONTINUITY
- TEST456 - POLY SNAKE TO POLY COMB LEAKAGE @ 50mV
- TEST457 - POLY SNAKE TO POLY COMB LEAKAGE @ 5.0V
- TEST458 - POLY SNAKE/COMB TO ISLAND LADDER LEAKAGE @ 50mV
- TEST459 - POLY SNAKE/COMB TO ISLAND LADDER LEAKAGE @ 5.0V

- ***DEVICE-44***

Row3 Col21

Top = Metal1 Serpentine thru Metal1 Comb and Poly Ladder

- TEST460 - METAL1 SNAKE CONTINUITY
- TEST461 - METAL1 SNAKE TO METAL1 COMB LEAKAGE @ 50mV
- TEST462 - METAL1 SNAKE TO METAL1 COMB LEAKAGE @ 5.0V
- TEST463 - METAL1 SNAKE/COMB TO POLY LADDER LEAKAGE @ 50mV
- TEST464 - METAL1 SNAKE/COMB TO PPLY LADDER LEAKAGE @ 5.0V

Bottom = Metal2 Serpentine thru Metal2 Comb and Metal1 Ladder

- TEST465 - METAL2 SNAKE CONTINUITY
- TEST466 - METAL2 SNAKE TO METAL2 COMB LEAKAGE @ 50mV
- TEST467 - METAL2 SNAKE TO METAL2 COMB LEAKAGE @ 5.0V
- TEST468 - METAL2 SNAKE/COMB TO METAL1 LADDER LEAKAGE @ 50mV
- TEST469 - METAL2 SNAKE/COMB TO METAL1 LADDER LEAKAGE @ 5.0V

- ***DEVICE-45***

Row3 Col18

Top = P+ Island Contact Chain, Contacts = 0.8μm

- TEST470 - TWO POINT RESISTANCE P+ ISLAND CONTACT CHAIN (0.8)

Bottom = N+ Island Contact Chain, Contacts = 0.8μm

- TEST471 - TWO POINT RESISTANCE N+ ISLAND CONTACT CHAIN (0.8)

- ***DEVICE-46***

Row3 Col19

Top = Metal2 - Metal1 Via chain, Vias = 1.0μm

- TEST472 - TWO POINT RESISTANCE METAL2 - METAL1 VIA CHAIN (1.0)

Bottom = Metal1 - Poly Via chain, Vias = 1.0μm

- TEST473 - TWO POINT RESISTANCE METAL1 - POLY VIA CHAIN (1.0)

- ***DEVICE-47***

Row1$^{1/2}$ Col20 (80μdownfrom Row 1!)

Top = P+ Island Contact Chain, Contacts = 0.8μm

- TEST474 - TWO POINT RESISTANCE P+ ISLAND CONTACT CHAIN (0.8)

Bottom = N+ Island Contact Chain, Contacts = 0.8μm

- TEST475 - TWO POINT RESISTANCE N+ ISLAND CONTACT CHAIN (0.8)

- ***DEVICE-48***

Row3 Col20

Top = Metal2 - Metal1 Via chain, Vias = 1.0μm

- TEST476 - TWO POINT RESISTANCE METAL2 - METAL1 VIA CHAIN (1.0)

Bottom = Metal1 - Poly Via chain, Vias = 1.0μm

- TEST477 - TWO POINT RESISTANCE METAL1 - POLY VIA CHAIN (1.0)